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REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION / AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S): ARO 26846.1-PH-CF
6a. NAME OF PERFORMING ORGANIZATION: IEEE Lasers and Electro-Optics Society	6b. OFFICE SYMBOL (If applicable)
6c. ADDRESS (City, State, and ZIP Code): Piscataway, NJ 08854	7a. NAME OF MONITORING ORGANIZATION: U. S. Army Research Office
	7b. ADDRESS (City, State, and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211
8a. NAME OF FUNDING / SPONSORING ORGANIZATION: U. S. Army Research Office	8b. OFFICE SYMBOL (If applicable)
	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: ARO MIPR 133-89
8c. ADDRESS (City, State, and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211	10. SOURCE OF FUNDING NUMBERS

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification): Workshop on III-V Integrated Optoelectronics

12. PERSONAL AUTHOR(S): Robert T. Wangemann (principal investigator on project)

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM 3/20/89 TO 3/19/90	Jan 1990	

16. SUPPLEMENTARY NOTATION: The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

17. COSATI CODES		
FIELD	GROUP	SUB-GROUP

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number): OEIC Technology, OEIC Devices, Workshop, Materials, Opto Electronic Integrated Circuits (OEIC)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

A Workshop was held for the purpose of bringing together researchers with a broad range of interests in OEIC and related technologies. The objecive was to review the current status and future prospects for OEIC devices, as well as related materials and materials processing technologies. This report summarizes the discussions that took place and highlight some of the conclusions drawn. The report is divided into six sections covering: emerging systems requirements, materials growth and processing for OEICs, state-of-the-art discrete components, a review of the current status of OEIC research devices, and a discussion of the conclusions of the Workshop.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code) / 22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

WORKSHOP REPORT

WORKSHOP ON III-V INTEGRATED OPTOELECTRONICS

MARCH 28-30, 1989
MARINER'S INN
HILTON HEAD, SOUTH CAROLINA

Supported by:
National Science Foundation
Air Force Office of Scientific Research
Labcom, Harry Diamond Labs
Rome Air Development Center
Office of Naval Research
Army Research Office
Defense Advanced Research Projects Agency
IEEE Lasers and Electro-Optics Society

Managed by:
IEEE Lasers and Electro-Optics Society

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This workshop report was submitted to the *Journal of Lightwave Technology* as an invited paper.

1. Introduction

Opto Electronic Integrated Circuits (OEICs), circuits that monolithically integrate optical and electrical components on a single semiconductor chip, represent a device technology with potential to meet a broad range of future telecommunication and computing systems needs. As for the case of integrated electronics, monolithic integration offers significant advantages over hybrid circuits in compactness, reliability, possible performance improvements resulting from reduced parasitics, and potentially significant reductions in cost, particularly in the case of arrays. However, despite these many potential advantages, to date OEICs have not outperformed hybrid circuits performing similar functions. This is generally recognized to be due to the difficult materials and materials fabrication challenges presented by integration of very different devices on a single chip.

On March 28–30, 1989, a Workshop was held for the purpose of bringing together researchers with a broad range of interests in OEIC and related technologies under the sponsorship of the IEEE LEOS Society and a number of government agencies with an interest in optoelectronic technologies including: The National Science Foundation, the Air Force Office of Scientific Research, the Army Research Office, the Defense Advanced Research Projects Agency, the Rome Air Development Center, the Army Labcom-Harry Diamond Labs, and the Office of Naval Research. The objective was to review the current status and future prospects for OEIC devices, as well as related materials and material processing technologies. In this report we summarize the discussions that took place and highlight some of the conclusions drawn. The report is divided into six sections covering: emerging systems requirements, materials growth and processing for OEICs, state-of-the-art discrete components, a review of the current status of OEIC research devices, and a discussion of the conclusions of the Workshop. The authors would like to acknowledge the contributions of the workshop participants for making this report possible.

2. Systems Needs for OEICs

2–1. Introduction

Research on OEICs is rooted in advances made over the past decade in the design and fabrication of discrete optical and electronics components using GaAs and InP, and their lattice matched alloys, AlGaAs, InGaAsP, and InGaAs. The match between bandgap energy of the InP based materials and the low loss optical fiber transmission windows at 1.3 and 1.5 μm has focused optoelectronic components research for fiber telecommunications systems on InP-based materials. GaAs and its related alloys represents a more mature material system in terms of research experience on growth and processing of complex material and device structures. These wider bandgap materials have been widely studied for high speed electronic and microwave applications and for optical components such as lasers for non-fiber applications including optical disc readers and communications systems employing free space propagation, or requiring only limited fiber runs.

Continuing advances in device design and fabrication, as well as in material growth and processing technologies, are providing the technology push to meet the research challenge represented by OEIC devices. At the same time, as optoelectronic components are being incorporated into communications and computing systems there is a technology pull for OEIC innovation to satisfy the demanding requirements of advanced systems. In this section we discuss some of these emerging systems applications.

2–2. Telecommunications Systems

For more than a decade, optical device research for telecommunications has been dominated by long haul, point-to-point transmission where the bit-rate distance product has been a key figure of merit. Todays commercial fiber systems operate at up to 1.7 Gbits/s, with capacities to 5 Gbits/s becoming available and research experiments pushing beyond 10 Gbits/s. These high bit-rate, point-to-point systems are characterized by relatively low optoelectronic component counts, so that cost per subscriber-circuit for components is not a critical issue.

To a considerable degree todays telecommunications systems research is looking beyond this limited point-to-point application and is aimed at creatively exploring ways to extend optical technologies into the subscriber loop where fiber offers the possibility for services greatly expanded over what is currently available with copper wire. For these applications it is envisioned that each subscriber would have access to information at rates up to 150 Mbits/s, compatible with switched digital HDTV signals for example [1, 2]. There is also growing interest in using fiber for broadcast cable TV distribution as well [3].

Underlying this research thrust is the recognition that, at the bit-rates required to support a single subscriber, the optical bandwidth of single mode fibers can support thousands of channels. The challenge for systems designers is to develop architectures that allow efficient switching of optical signals as they are routed from multi-gigabit trunk lines to these individual subscribers. In this subscriber loop environment, remote from the controlled environment that characterize central switching offices, the use of complex electronic switching to route broad-band signals to individual subscribers presents a challenge that can possibly be met by passive photonic technologies. One approach is to develop cost effective OEICs to simplify the implementation of Time Division Multiplexing (TMD) systems. The more advanced approach is to take advantage of wavelength selectivity to realize systems based on Wavelength Division Multiplexing (WDM) [4], a systems approach that mimics in the frequency domain TMD systems. In such a system, specific wavelengths are assigned to separate channels, much as time slots are assigned in TDM, for transport or broadcast of large numbers of signals via fiber while using wavelength selectivity to sort and route individual signals to their final destinations. One such system for routing or switching based on WDM is illustrated in Fig. 1 [4]. Future systems are expected to make extensive use of coherent techniques to select received signals in a mode similar to today's radio/TV broadcast systems [2]. It should however be noted that cost effective TDM network based on high speed OEICs will probably be first to be implemented.

The key feature of these research architectures is that they rely on intensive optoelectronic interfacing. For successful implementation of these schemes three key challenges exist for device researchers; first, to provide lasers with precise frequency control; second,

to develop wavelength-selective receivers; and third, provide these interface components at a cost, per customer-served, compatible with what the markets for services such as broadband ISDN and digital HDTV are able to support. These performance challenges can be met with hybrid components, and in fact, many of the present research demonstrations rely on hybrids. However, successful replacement of these hybrids by low cost, reliable OEICs would greatly enhance the progress of this work. Successful implementation of TMD and WDM switching with OEICs, as envisioned here for communications applications, could also impact directly on massively parallel computer systems where the input/output ports illustrated in Fig. 1 might represent individual processor and memory boards [6].

2–3. Computing Systems

As computing environments evolve towards the type of distributed network illustrated in Fig. 2, with data processing and data base sharing among remote locations, overall operating efficiency increasingly relies on the efficiency of interconnection links. Even when the spans being bridged are quite short the physical size and complexity of wire and cable, as well as their high frequency loss and limited bandwidth, place severe restrictions on the distance over which repeaterless connections can be made. For some time a variety of new approaches have been considered based on optical links as a means to achieve high bandwidth, low loss interconnection for these applications. This represents another area where OEICs could have significant impact.

While in many respects the technology challenges of optical data networks resemble those of telecommunication networks, in detail their requirements can be quite different. For one, the relatively short distances characterizing many data network interconnections translates to relative insensitivity to fiber transmission losses (or dispersion), at least for bit-rates on the order of $\sim$ Gbits/s and distances on the order of a kilometer. As discussed in Section 2-1, advances in optical communication device technologies have been based on InP materials oriented to long wavelength operation taking advantage of the low loss properties of fiber for long distance communication systems. For many data links, short interconnect spans allow for considerable flexibility in the choice of operating wavelength, and in particular the use of GaAs short wavelength ($\lambda \sim 0.8$) optics and electronics (ion-

implanted FETs). Given the more advanced state of development of GaAs integrated electronics, this material system is in excellent position to immediately meet many of the challenges of short distance optical interconnections. The work of a number of groups reporting GaAs-based OEICs supports this, with a few demonstrations of very high levels of integration [7,8,9].

Another critical aspect of data networks relates to the bursty nature of data communication channels, characterized by rapid transfer of large blocks of information between remote points via connection paths that may change during the course of computation. The challenge is to create low cost interfaces that can efficiently couple components, such as processor and memory bank, and which exhibit fast set-up time (nsec), even faster data transfer rates (Gbits/s), and which are compatible with existing data processing equipment standards.

This final point has been emphasized by Crow, et al, of IBM [9] who point out that if OEICs are to successfully compete with an all-electronic approach the optical and electronic devices making up OEICs, and the circuit functions implemented, must represent a robust technology that can compete on the basis of cost and performance with todays electronic ICs, while also being as compatible as possible with standard IC packaging. The materials systems and growth techniques need to be as simple as possible. The optical and electronic device structures need to be simple and tolerant to the process variations expected in IC processing. Fig. 3 illustrates the functional characteristics of a GaAs computer interface OEIC chip reported by Crow and co-workers [9] which incorporates many of these features. For insertion into a practical computer system, this circuit has been designed to meet the following requirements:

- high speed, capable of multi-Gbit/s, with relatively high complexity (10K transistors/chip),
- capable of operation in a noisy environment, BER$< 10^{-15}$ in the presence of noise levels of up to 100 mV,
- high reliability, failure rate $< 0.01\%$ per khrs for an entire link, for over 10^5 hours at 50°C,

- redundancy in critical paths with transmission error correction capacity,
- compatible with existing computer interface technologies; packaging, power supply requirements and silicon interface, and
- be competitive, i.e. satisfies a market niche with market volume in excess of one million devices per year to ensure low cost and ready availability.

This list provides a concise summary of the goals for any OEIC component. It is important to note that with continued evolution of optical techniques for data transmission many of the systems architectures being considered for telecommunications applications, such as WDM, may also find use in computing environments and vice versa.

Even at chip level, advances over the past decade in silicon VLSI technologies have made possible todays signal processing and computer IC chips incorporating up to a million devices and operating at clock rates in excess of 150 Mbits/s. This expanded chip level processing capacity has translated to increased demands on chip I/O ports, with the number of connections to high performance chips exceeding 200, and projected to reach over 500 in the near future. Within silicon technology this requirement for high speed transfer of data has given rise to electronic circuit designs that mix device technologies, i.e. BiCMOS. The incorporation of bipolar devices with traditional CMOS circuits can provide required current drive for coupling off-chip but an innovative OEIC alternative, that might offer even greater flexibility, has been proposed by researchers at David Sarnoff Research Center. Their proposal, which is typical of many suggestions for how OEICs might serve to meet this chip-to-chip interconnection challenge, replaces the current drivers required for electrical interconnects with optical components as illustrated in Fig. 4 [10]. The Sarnoff researchers propose to deposit GaAs directly onto selected areas of the silicon wafer, taking up about the same area as present metal wire bonding pads, to provide material for on-chip OEICs. They envision a small scale OEIC incorporating a laser transmitter providing optical interconnection access and high speed multiplexer circuits to serialize the many parallel data streams operating at the lower clock rate of the silicon components. Given the high speed capabilities of the GaAs optoelectronic components, this approach could reduce the required number of high performance I/O ports by more than an order of

magnitude. Related technologies can provide on-chip receiver circuits performing optical detection and demultiplexing. Similar applications of GaAs on Si, incorporating GaAs LEDs with Si-MOS driver circuits, have been reported by researchers at Lincoln Labs [11].

2–4. Military Systems

Military requirements for communications and computing represent some of the most demanding for technology and this has been reflected in early interest by DOD agencies in a host of advanced optoelectronic device applications including support for some of the pioneering work in GaAs OEIC's. Bit rates for military communications match those found in typical telecommunications systems; 50 Mbits/s for battle field management, 200 Mbits/s for the denser traffic typical of an aircraft with its large number of sensors and other instrumentation requirements, and more than one Gbit/s for the LAN/Local Loop like environment typical of shipboard operations. In most respects these systems are quite compatible with non-military telecommunications, but often the applications translate to some rather unique systems considerations, such as the simple replacement of copper cable with fiber to reduce weight for field deployed telephones or aircraft wiring.

Computing in military environments supports very high speed, real time decision making which creates requirements for rapid interconnection of multiple processors with distributed sensors and data-bases, under conditions where individual components may be quite physically separated so that fiber links can provide a real advantage. In addition to the challenges of high speed digital processing, which parallel many non-military applications, military computing also includes high speed signal processing systems for pattern recognition and related functions. These systems have been shown to make innovative use of optoelectronic components with holographic signal distribution and optical signal processing in neural networks (see Fig. 5) representing one such "optical computing" application for which optical components are integral to the computation process. Of course successful implementation to meet military needs would result in many non-military applications for this technology.

The distribution of microwave signals by optical fiber represents still another potentially major application for OEICs in military systems. In this instance it is envisioned

that advanced antenna systems making use of phased array techniques will require very large signal distribution networks typical of that illustrated in Fig. 6. The use of optical techniques to distribute and control the phase and amplitude of microwave signals could greatly enhance the efficiency, size, weight, cost and performance of these systems. The development of efficient microwave signal distribution by optical fiber creates the possibility of achieving efficient unconventional antenna structures such as "smart skin" where individual radiating elements would conform to the contour of an aircraft and the "antenna's" directional properties would be determined by control of the phase of emission from different parts of the aircraft. Apart from the very large number of devices required to achieve an efficient system (~10,000 individual radiators), the microwave operating frequency of the antenna is envisioned to be in the 50–90 GigaHertz range, creating challenges of device researchers to fabricate optoelectronic components capable of modulation at these high frequencies. It should be mentioned that some high frequency electronic components are already becoming available. They are being developed under the auspices of the Department of Defense (DOD) mimic (millimeter wave ICs) program. This program is funded for 7 years at the level of $500 million to develop high speed GaAs circuitry.

In these military applications the potential for enhanced performance to be gained by creative incorporation of optoelectronic components is comparable to that anticipated for non-military markets, and again integrated OEICs could contribute significantly to reduced systems cost and improved reliability.

2–5. Market Size

The initial applications for OEICs will be at the high end of the markets discussed here: supercomputer interconnects and telephone switching centers, where the reduced size and complexity of interconnections made possible with integrated devices will provide the technology advantages for OEICs to compete with hybrids. In this competition, OEICs have three advantages:

1). reduced size, an advantage that is truly significant for applications where optoelectronic components are required or where the high speed capabilities of optoelectronic devices allow for significant reduction of interconnect lines by TDM. This also results

in lower packaging costs and improved noise immunity,

2). reduced cost of production, considering that cost of integrated devices have historically decreased significantly as the number of devices produced increases, and,

3). reliability, again experience with integrated components indicates that once a fabrication process is established, the reliability of the finished components is enhanced over hybrid versions as the number of wire bonds and related mechanically weak points in the circuit are reduced. A further aspect of reliability is enhanced noise immunity.

To be truly successful, the market for OEICs must be large enough to sustain the investment in production. A generic OEIC, such as the chips illustrated in Fig. 4, which finds wide application, could then support further developments of the technology base. For the three types of systems considered here, each represents a market potential for over a million devices per year filling the need for OEIC interface chips for every telephone subscriber, every telephone line at the switch, every PC/workstation tied to a network, and every aircraft, ship and most vehicles where optical components can enhance the distribution of information. For uniquely military systems application such as the phased array radar systems discussed here, a single antenna may represent 10,000 elements which can be multipled by a market of a few hundreds of systems to yield a potential market of more than a million OEIC devices.

3. The Role of Materials in OEICs

Initial OEIC technologies will rely on todays materials technologies, ion-implanted GaAs electronics and selective growth of material for optical sources, but as experience with integration evolves, OEIC applications represent a technology application for the most advanced materials synthesis and materials processing techniques. Fig. 7 illustrates the variation in bandgap energy with lattice constant for representative binary compounds and their alloys. Vertical lines on this plot represent lattice matched material compositions. There are two broad areas of materials synthesis which are very relevant to the development of OEICs. The first is the growth technique needed to realize the complex lattice-matched heterostructures required, and the other, to a lesser extent, is mismatched hetero-epitaxy. Although significant progress has been made in the immediate past in both

areas, much more understanding of the III-V materials growth and processing, in its control and uniformity, and in its influence on device parameters is required before acceptable yields can be realized from OEICs.

Among the techniques commonly used to develop optoelectronic devices and OEICs, the methods of MBE and MOCVD have emerged as the strongest contenders. While LPE is still widely used to produce discrete buried heterostructure lasers, this technique is very difficult to apply to the preparation of transistor structures. MBE can produce high quality lasers with interfaces abrupt on the atomic scale. It can also be used to achieve extremely high doping levels. These growth characteristics are crucial for high performance transistors. MOCVD, on the other hand, offers the possibility of extremely long minority carrier lifetime (low non-radiative recombination rates), ease of regrowth properties essential for the fabrication of laser structures and high production throughput. However, it is not clear if structural and electrical characteristics of heterostructures and quantum wells prepared by MOCVD approach that achieved by MBE.

Gas-source MBE (GSMBE) or metalorganic MBE (MOMBE) [12, 13] integrates the techniques of MOCVD and MBE and may prove to be extremely important for optoelectronics and OEIC development. Impressive results on materials and heterostructure characteristics have been reported in the recent past and in particular, in the performance of heterojunction bipolar transistors [14]. GSMBE appears to be well-suited to the important In-Ga-As-P system where it permits extreme precision in dimensional control and simultaneous extremes in doping, not currently available by other growth methods. For example, p-type doping levels with Be of over $5 \times 10^{20}\text{cm}^{-3}$ have been demonstrated [15]. This capability is important for the design of the base region of HBTs. These capabilities also enable ballistic motion of carriers through the base, thereby improving the dynamic characteristics of these devices. Values of f_T =165 GHz have been demonstrated in InP/InGaAs HBTs grown by GSMBE. High speed and high current capabilities of HBTs makes them attractive for OEIC development. However, it is important to explore regrowth possibilities and characterize the regrown interfaces.

In the area of lattice mismatched heteroepitaxy, one of the two possible alternatives

are pseudomorphic materials, where the grown layers are within critical thickness limits and therefore coherently strained. In the other form of mismatched epitaxy, the strain is generally larger, resulting in high dislocation density, and the challenge is the control of dislocation propagation into the active regions. The most studied system is GaAs on Si, although more recently interesting results have been reported on InP and InGaAsP optoelectronic devices on Si. There are several potential and obvious advantages in this type of heteroepitaxy as well as a number of difficulties.

In the critical area of dislocation control, the more recent experiments on patterned growth appears promising [16]. Dislocation have, in general, been a limiting factor in the development of III-V devices on Si substrates. While reasonable quality HBTs ($f_T = 35GHz$) have been fabricated [17], the noise performance of HEMTs and MESFETs is not currently as good as that obtained from lattice matched materials. It is perhaps more important to explore the limitations of optoelectronic devices on Si, since a likely scenario in OEIC development is the integration of "pockets" of III-V optical devices in a "sea" of Si VLSI. GaAs/AlGaAs lasers on Si substrates with $I_{th} \sim 35mA(30 - 40kA/cm^2)$ and a modulation bandwidth of $\sim$ 2GHz have been reported [18]. However, reliability of these devices remains a serious issue.

The quality of InP on Si also looks promising. Epitaxial layers grown by LP-MOCVD show good luminescence efficiency and narrow linewidth [19]. InGaAsP/InP/GaAs/Si buried ridge lasers with I_{th} =45 mA ($\sim 4kA/cm^2$) have been reported. These degrade about 5% in 5 hours of operation [20]. The integration of 10 NMOS FETs in three stages with LEDs have also been reported [11].

Another possible scheme for heteroepitaxy is the growth of GaAs on InP substrates [22]. This allows the integration of GaAs electronic devices with InP or InP-based light sources and detectors. Encouraging results have been demonstrated both in electronic and opto-electronic devices. GaAs lasers on InP exhibit $I_{th} \simeq$ 300 mA [23]. GaAs MESFETs based laser drivers have been integrated as drivers with InGaAsP lasers [24], Figure 8. A rather unusual technique, which may impact OEIC development by allowing combinations of completely dissimilar materials, is a lift-off method in which the layers grown on the lat-

tice matched substrates are selectively etched off and placed on other (lattice mismatched) substrates [25]. The thin films, which may contain electronic, optoelectronic and magnetic devices (and circuits) then adhere by van der Waals bonding.

Devices in which the active region is coherently strained have gained importance in the recent past. Some of the best high-frequency and low-noise transistors have used such strained layers [26]. Similarly, extremely low threshold currents have been realized with InGaAs/AlGaAs strained active layers. Until recently, strained layers were looked upon as a means to alter the bandgap and band offsets. It is evident now that, in the quantum size limit, biaxial strain can significantly alter the band structure and associated transport properties, opening up new device possibilities [27]. For example, biaxial compressive strain in quantum wells can lower the in-plane hole effective masses to values nearly equal to those of electrons [28], as illustrated in Fig. 9. Similarly, biaxial tensile strain offers the possibilities of enhancing the carrier effective masses and absorption coefficient.

It should be of course realized that the great progress in OEIC development has been made with GaAs- and InP-based lattice-matched materials. These will remain dominant for the highest performance OEICs. Special techniques such as regrowth, selective regrowth, and small-area growth need to be developed and characterized more fully. Recognizing the more mature status of GaAs materials technologies and the existence of a substantial GaAs electronic IC technology it is likely that for local area networks, computer interconnections, optical information processing and automotive applications, GaAs-based (or GaAs on Si) OEICs will be most useful. InP-based materials technologies, particularly for electronic applications, lag at least a decade behind GaAs, but given the success of InP materials for long wavelength optical devices these materials seem most promising for longer distance ($> 10\ Km$) fiber-optic communications.

4. Limits of Size and Processing of Future OEICs

4.1 Introduction

While the fabrication of some present day OEICs does not appear to be hampered greatly by materials and device processing, there appears to be a strong consensus that cur-

rent techniques will not be sufficient in the near future. These future *OEICs* are expected to be based on quantum well structures patterned on a very fine scale and to very tight tolerances. Present day processing techniques are adequate, in the research sense, when transverse dimensions on the order of 100 nanometers or more are required. These dimensions are already standard in high speed FET gates. For the second generation OEICs, new patterning techniques will have to be established in order to reach the 10 nanometer range. Quantum mechanical two-dimensional confinement effects will then become important in the operation of optical and electronic devices.

Two distinct directions are emerging in nanofabrication science. The first pushes the limit of very fine scale electron beam lithography to achieve some of the smallest devices possible [29]. The second approach is to incorporate the device processing into the material growth environment [30]. This necessitates the development of vacuum compatible lithography [31] and much greater sophistication in the epitaxial growth on patterned and tilted substrates [32].

4.2 Fabrication of Nanostructures

Shrinking the size of semiconductor devices has in the past resulted in significant performance improvements and revealed new device physics. This trend is expected to continue as lateral dimensions on the order of 10 nm are achieved. These dimensions are currently available only through electron beam lithography. This writing process is resist limited and while e-beam spot sizes of 5 nm are achievable, the features written are typically a factor of 3–4 larger as a result of electron scattering and limits on resist resolution. Even more critical is the problem of transferring the lithographic pattern to the underlying semiconductor structure. Small sizes demand very faithful replication of the e-beam written pattern, high degree of anisotropy and, above all, damage-free surfaces. Considerable attention has therefore been devoted to various low energy dry etching processes. Ion beam assisted etching has been used extensively because of its relative simplicity and low ion beam energy resulting in low sidewall damage. This process has been used for preparation of high quality laser facets and optical waveguides. The question of damage in the limit of very small sizes, down to 60 nm quantum dots, has been recently studied in careful detail

[33]. These results are shown in Fig. 10. The cathodoluminescence measurements on such GaAs structures with etched sidewalls showed intensity decreasing at the same rate as the surface to volume ratio indicating normal surface recombination velocity limits. Similar results have been obtained in 30 nm diameter quantum dots of InGaAs/InP [34] in which the surface recombination velocity is at least a factor of 100 smaller. In order to maintain optical and electrical quality of such small structures surface passivation techniques must be developed. Any technique which would result in buried structures of this type would also be of interest.

4.3 In-situ Processing

Most optoelectronic device structures are fabricated from structures consisting of planar epitaxial layers. These base structures are then patterned, using conventional processing techniques, to form active device mesas. The active regions are overgrown (buried) in a second epitaxial growth in order to provide current or optical confinement and to reduce the surface recombination velocity. Growth on patterned substrates, in order to create buried devices in a single step, is beginning to be explored. A good example is the preparation of GaAs/GaAlAs quantum well lasers grown in v-grooves etched in the substrates. The low growth rate on sidewalls provides quantum well structures which results in carrier and optical confinement to the bottom of the patterned structure. This has been used [35] to fabricate very high quality $I_{th} \sim 1mA$ buried heterostructure lasers in a single growth cycle. The technique can be readily extended to the preparation of laser arrays, passive waveguides with a very tight optical mode confinement, and the preparation of lower dimensional nanostructures.

Another possibility being explored is in-situ pattern formation. One possibility with this technique is to combine focused Ga beam writing and dry etching with MBE. Such combination of crystal growth and high precision patterning techniques can produce an efficient vacuum lithographic process [31, 36]. One variant uses low dose Ga implantation to effect localized damage in the surface of InP substrates. The etch rate of exposed regions is approximately a factor of ten larger than that in the remainder of the substrate. The dry etching removes the damage resulting from Ga implantation and dry etching conditions

can be adjusted to minimize surface damage. A schematic diagram of the apparatus and an illustration of the process sequence are shown in Fig. 11. This process produces surface steps as deep as 200-300 nm for the Ga dose of 10^{14} cm^{-2} and a spatial resolution of 0.2 μm, with a limit of less than 50 nm envisaged. The high quality of InGaAs/InP double heterostructures grown by gas source MBE on such in-situ prepared surfaces has been confirmed by a variety of optical and electrical measurements

4.4 Quantum Well Disordering

Significant advances have been achieved in the understanding and device applications of quantum well disordering (QWD). The process phenomenology is by now well known for the GaAs/GaAlAs material system and preliminary observations are being reported for InGaAsP/InP. Briefly, the idea is to accelerate thermally induced interdiffusion in quantum wells and barriers through implantation or in-diffusion of a variety of dopant species. The composition of the layers is arranged to assure that the interdiffusioned material has a larger effective bandgap than the lowest confined particle state of the original quantum well. The localized disordering can then be used to confine carriers to the desired regions of the quantum well. This has been demonstrated on a scale as fine as ~60 nm, [37]. Quantum well disordering has been used to fabricate very high quality, high power semiconductor laser arrays ($I_{th} < 50mA$ *and* $P_{out} = 250mW$) [38]. An elegant combination of laser beam activated layer desorption within the MOCVD growth apparatus and QWD has been demonstrated for laser wavelength control [39]. More recently lateral bipolar transistors in which the emitter and collector regions have been formed by QWD have been demonstrated. The device structure is shown in Fig. 12. This process allows for relatively straightforward monolithic integration of lasers and bipolar transistors [40].

5. State-of-the-Art Discrete Components

5.1 Transistors

The advantages of III-V compound semiconductor materials for high performance, high speed electronics are widely recognized. These advantages stem in part from the versatile device structures made possible by advanced heteroepitaxy and in part from excellent

electrical characteristics of lattice matched heterostructures and the superior velocity field characteristics of the underlying materials as illustrated in Fig. 13. In detail, carrier velocity varies significantly through a device, but for a given type of device, materials with high low-field mobility and high peak velocity (i.e. InGaAs) generally exhibit lower parasitic resistance and greater current carrying capacity. The figures of merit for transistor high speed performance, such as unity gain cutoff frequency f_t, reflect these considerations so that devices with active regions composed of materials with good transport properties, such as InGaAs, are expected to outperform transistors fabricated using other materials [41].

To appreciate the advantages of heteroepitaxial structures, consider the variety of field effect and bipolar transistor types currently being investigated for various electronic applications illustrated in Fig. 14. Generic forms of these devices are shown in Fig. 15. HBTs have high current drive capacity and can be packed with relatively high density. They exhibit high transconductance for low voltage swings and, since their threshold voltage is determined by material bandgap energy, they exhibit very uniform threshold. FETs on the other hand have the advantage that they exhibit high input impedance, low parasitic capacitances, and do not suffer from charge storage in saturation [42].

Over the past years a number of variations on material structures to achieve high performance device operation have been explored. At present the structures of choice are remarkably similar regardless of the material system used as illustrated in Fig. 16a for HBTs and in Fig. 16b for FETs [43]. Enhanced HBT performance derives from the bandgap difference between base and emitter, and in some cases between base and collector. These differences allow for optimizing the doping of the various layers to achieve high efficiency for minority carrier injection while minimizing parasitic elements [44]. For FETs optimization is achieved in part by maximizing channel doping while minimizing carrier scattering, and this is currently best accomplished by using modulation doping and short gate lengths. Very high doping in the contact region is also critical. In addition to reducing gate capacitance, short gate length reduces effective carrier transit time, giving rise to improved high frequency performance.

Essential design principles for fabricating conventional high performance transistors have been understood for some time, but the actual realization of material growth and device fabrication techniques to achieve performance at the physical limits of the materials is still an active research topic. Applications of advanced epitaxial techniques to prepare material structures for InP/InGaAs transistors are only now emerging, almost a decade behind similar advances for GaAs. The low surface recombination velocity characteristics of InP and InGaAs surfaces contribute to enhancing the injection efficiency of the emitter-base junction [45]. See Section 3 for further discussion of materials issues. The electrical characteristics of InP/InGaAs HBTs are quite similar to those of silicon bipolar devices, allowing for the substitution of InP based HBTs for silicon devices in many ECL circuit designs [46].

Reflecting continuous rapid improvements in material growth and device fabrication technologies some very impressive high frequency devices have been recently demonstrated [47]. Fig. 17, showing the variation of f_t with gate length for state-of-the-art FETs, illustrates some of these results. Similar performance results have been reported for HBT structures [48], demonstrating that at least for discrete devices, well designed III-V transistors can meet the performance predictions based on their superior carrier transport properties.

Extending these discrete performance results to integrated circuits remains a challenge. At present the process for fabricating integrated circuits with more than a few dozen transistors rely on less aggressive device designs. For GaAs FET-ICs, ion implanted devices with gate lengths $> 0.5\ \mu m$ and more typically $1.0\ \mu m$, are the technology basis for a number of IC manufacturers and foundries. GaAs HBT-IC technologies remain primarily an advanced development topic, although circuits incorporating up to $\sim$1000 transistors have been reported.

At present IC technologies using InP/InGaAs materials remain a research topic with no FET circuits larger than a few transistors being reported. Research results substituting InP/InGaAs/InAlAs for GaAs/AlGaAs in HBT/FET-IC designs look promising [49].

In general, for technology comparisons, silicon bipolar circuits have been demonstrated

to operate at up to $\sim 0.5 f_t$ for discrete transistors while III-V ICs operate at only $\sim 0.25 f_t$. This translates to $\sim 10 - 15$ Ghz for very high performance silicon and $\sim 20 - 30$ Ghz for III-V's [50]. A major factor contributing to the lower operation frequencies of III-V circuits is limited experience in the design of ICs to operate at these frequencies where parasitic effects of interconnects and packaging are very significant. Nevertheless, properly designed GaAs ICs have been demonstrated to have as much as a factor of ten advantage in power at the same operating speed over silicon circuits [49, 51].

5.2 Lasers

The design of semiconductor lasers reflects some of the most advanced material science and device processing technologies. Modern semiconductor lasers rely on heteroepitaxial structures to create carrier diffusion barriers defining the active region vertically and laterally. In addition, these buried heterojunction barriers also provide optical guiding to control the transverse optical modes of the laser. In the simplest design, optical feedback is provided by reflections from cleaved facets which provide little in the way of longitudinal mode control. The introduction of distributed reflections from grating structures can greatly enhance frequency control, which in combination with external reflectors, allows for high Q cavities having finer control over operating wavelength [52, 53]. In today's advanced InGaAs/InP laser devices, such as the one illustrated in Fig. 18, external cavities have been replaced by monolithically integrated waveguides, and, by providing separate current injection, it is possible to take advantage of free carrier induced changes in index to fine tune the operating frequency of the laser [54, 55]. With good control over the epitaxial growth of the device structure, it is now possible to fabricate InP based lasers with threshold current densities below 1000 Amps/cm^2 ($I_{th} \sim 10$ mA) [56]. GaAs/GaAlAs lasers exhibit threshold current densities < 200 Amps/cm^2 ($I_{th} < 1$ mA) [57]. Differential efficiencies greater than 80%, that is above threshold more than 80% of the electrical power delivered to the laser is emitted as light, can be achieved and this very high electrical efficiency makes semiconductor lasers very attractive for such applications as optical pumping of solid state lasers [58] and the distribution of microwave signals [59].

For some time it has been recognized that by reducing the thickness of the active region

to form a quantum well, the effective density of states at the bandedge could be reduced, with corresponding reduction in threshold current density required to achieve population inversion [60]. With reduction in the dimension of the active volume, the quality of material interface becomes critical to realizing the advantages of quantum confinement. Within the last year GaAs Quantum Well (QW) laser designs have been demonstrated that achieve this goal using both traditional device structures [61] and also vertical geometries in which high reflectivity, integrated mirrors are used to achieve high Q cavities [62, 63]. For these devices threshold currents have been shown to be as low as a milliampere. Future improvements are expected to yield further reductions in threshold currents for these devices making possible efficient one and two-dimensional array operation for a variety of applications [64, 65].

Reduced current drive is advantageous for many applications, as for example where the laser driver circuit has limited current drive capabilities, or in laser arrays where heat generated in driving one laser can adversely influence the threshold for adjacent devices, and for these reasons QW lasers have been recognized as having advantages for OEIC applications [64]. Low threshold is also important for high speed modulation applications where it is desirable to operate well above threshold $I > 10\ I_{th}$ to take advantage of very rapid stimulated recombination of injected carriers [66]. A further advantage of QW lasers is the control over optical gain spectra available. Recent results have demonstrated that extended tuning range for QW lasers is possible relative to the more usual laser structures [67].

5–3. Photodetectors

Photodetector designs range from simple photoconductive devices which rely on detecting optically excited carrier flow between ohmic contacts, to advanced Separate Absorption and Multiplication-Avalanche Photodetectors (SAM-APD) that take advantage of complex heterostructures to separate the photodetection process (InGaAs) from the avalanche multiplication process (InP p-n junction) to achieve better low noise performance [68]. Perhaps the most ubiquitous photodetector for the wavelength range of interest for OEICs is the simple p-i-n diode. In this design it is desirable to confine the light absorption

to the high field "i" region formed in the diode depletion region to insure rapid sweep-out of the photoexcited carriers [69]. For applications in high performance systems the key parameters of p-i-n diode design are reduced capacitance, "i" layer thickness large enough to efficiently absorb the incident light ($\sim 1 - 2\mu$m) and low dark current.

The difficulties associated with integrating pin diodes with FET amplifiers in OEICs has given rise to a new approach to photodetector design based on back-to-back metal-semiconductor Schottky diodes forming what is known as an MSM detector. As illustrated in Fig. 19 this metal-semiconductor structure can be fabricated at the same process step as the FET gate metallization thus greatly simplifying the process of integrating photodetectors with FETs [9,70]. From the point of view of minimizing dark current, Schottky diodes [9,70] are not generally as effective as reversed biased p-i-n junctions, but dark currents less than 10 nanoamps have been demonstrated. A major advantage of MSM detectors is the fact that their capacitance is typically significantly less than that of a p-i-n device of the same area [71] allowing for higher gain amplifiers and higher overall receiver sensitivity at a given bandwidth than possible with a pin photodetector. While useful for reducing capacitance in photoreceiver circuits this property does not translate directly into short response speed due to the complex transit time associated with the electric field distribution in the photosensitive region beneath the MSM contacts [72]. The technology for Schottky metal on GaAs is relatively well established but it is only recently that comparable devices have been demonstrated using InGaAs [73a,73b,74].

Just as in the case where integration of laser active region with waveguide structures greatly enhances the design options for laser structures, the integration of photodetecting devices with waveguides has some advantages [75] and Fig. 20 illustrates one such application [76a]. The introduction of wavelength selective elements into the waveguide should allow these devices to operate as "tuned" detectors. In fact for some integrated applications, to a considerable degree, the "integration" will be predominately optical and for these applications the acronym "PIC" for Photonic Integrated Circuit [76b] may be more appropriate than "OEIC".

6. OEIC Transmitters and Receivers

The success of optical communication has accelerated the research on high capacity data handling systems. It is expected that the monolithic integration of optical and electronic components on the same chip will ultimately lead to ultra-high speed, high sensitivity, compactness, reliability, and low cost (or some combination of the above). Since the pioneering work by Yariv and co-workers [77] on the monolithic integration of optical and electronic components on the same chip, there have been numerous contributions that have been reported in the literature [78-90]. So far, both GaAs and InP materials have been used to demonstrate different types of OEIC's. The high electron drift velocity and high electron mobility of these systems, as well as the ability to form heterojunctions exhibiting high quantum efficiency, combine to make these materials highly desirable for high-speed electronic and optoelectronic devices. The complexity of GaAs integrated circuitry is very advanced and the integration of tens of thousands of components has already been reported. It needs to be stressed that the number of elements associated directly with the optical function of the circuit remains quite small. Typically the majority of the circuitry is devoted to electronics, including all the logic and decision functions. This is particularly true when an electronic multiplexer/demultiplexer, automatic gain and power control, and clock extraction circuitry, are integrated, as illustrated in Fig. 21. Research on OEICs transmitters is typically focused on a level of integration limited to a current amplifier driving a laser (and possibly a power monitoring photodiode) and the laser. For receivers, the level of integration is limited to an amplifier following a detector in a receiver. Only recently, multichannel transmitter and receiver array OEICs have been demonstrated [78]. At these levels of integration, OEICs represent a direct replacement for hybrid and flip-chip [91] circuits performing similar functions and OEICs compete with hybrids for these applications principally on the basis of cost and reliability. Integration offers even greater potential advantages in the areas of arrays of optoelectronic devices where integration will allow greatly simplified processing and packaging, as well as, offering the possibility for on chip optical signal processing using active and passive photonic components (Fig. 22). Optical waveguides and two-dimensional arrays of lasers will be integrated on the chip. OEICs will make possible entirely new system functions via monolithic integration. These functions include optoelectronic gating, wavelength multiplexing and demultiplexing, op-

tical interconnections between chips and within a chip, two–dimensional optical switching and memory elements based on optical bistability. The speed and noise performance of optoelectronic devices will be significantly improved by the reduction in parasitics resulting from integration.

Here we review the current status of OEIC technology. There are two basic structures for creating a monolithically integrated optoelectronic chip. One of these is a vertical structure (Fig. 23a) in which the epitaxial layers for both the optical and the electronic devices are grown in turn with the help of insulating layers to electrically isolate different devices. In such a structure, it is possible to integrate many compact devices and achieve three dimensional functionality. In practice, it is found to be difficult to grow sufficiently good insulating layers to minimize electrical coupling between components. A further shortcoming of vertically integrated structures is the nonplanar nature of the electrical interconnects between the photonic and electronic circuit components. The second structure of interest for OEICs is a more conventional two-dimensional horizontal structure (Figs. 23b,c,d,24) in which both optical and electronic devices are positioned roughly in the same plane over a semi-insulating substrate. This approach minimizes the capacitive coupling between the elements and, because of this, most recent investigations of OEIC's have taken this approach. However, processing becomes more complicated because of the need for subsequent growths, and because of the presence of surface steps. Typically the preparation of such an OEIC involves the following steps: a) well etching, b) epitaxial crystal growth, c) removal of unnecessary materials, d) ion implantation and activation, e) deposition of insulating dielectrics and diffusion of dopants, f) formation of Ohmic contacts, g) Schottky barriers, h) interconnections, and i) laser facet formation. It is difficult to carry out this complex process while maintaining optimized component performances.

Despite the potential advantages of OEIC's in reducing parasitics, it has been found in practice that the integration of both optical and electronic devices on the same chip necessitates some compromises in the performance of discrete components. Fig. 25 gives a performance comparison between hybrids and OEICs receiver sensitivity [92]. The source of the lower OEIC sensitivity comes largely from the functional and structural differences

between the optoelectronic and electronic devices being integrated. In an effort to planarize the process, optical devices are usually grown in an etched well and optical and electronic devices occupy different locations on the chip. As a consequence, interconnection yield deteriorates due to surface steps formed between optical and electrical components. This also makes fine line lithography difficult. Different material composition and doping parameters are required for optical and electronic devices. Lasers (HBTs) require fairly heavily doped active (emitter-base) regions, while FETs require tight control over the channel layer doping-thickness product. P-i-n photodetectors incorporate three distinct doped regions with very stringent requirements on the intrinsic region.

It is therefore important to search for new compatible component designs. The use of metal-semiconductor-metal (M-S-M) photodetectors is compatible with FET processing and greatly simplifies overall fabrication of an integrated photoreceiver [78, 80]. Another example of a planar compatible OEIC design based on quantum well disordering proposed by Fujitsu is shown in (Fig. 26) [93].

High-level-of-integration OEICs have already been demonstrated. A GaAs transceiver chip including 500 FET gates integrated with a photodetector and a laser and operating at 1Gbit/s has been reported by Honeywell [88]. At IBM, it was recently reported that GaAs OEIC receiver circuits based on an M-S-M detector with more than 8000 devices could perform deserialization, detection and clock recovery at rates close to 1 Gbit/s [9,80]. A 5 Gbit/s OEIC transmitter has also been demonstrated by Toshiba (Fig. 24) [94]. Researchers at Fujitsu demonstrated the impressive performance of a 4 x 4 optical switch at rates of order 1 Gbit/s [78]. This switch consists of a chip set comprised of a four-channel OEIC receiver, a 4 × 4 GaAs IC switch and a four-channel OEIC transmitter. The GaAs IC has more than 488 components integrated on a semi-insulating (SI) GaAs substrate. NTT and Fujitsu were among the first to use the MSM photodetectors for integration with GaAs MESFET's technology.

The material system that should be used for the next generation of OEIC's is still a matter of debate. So far, GaAs technology has offered the highest performance OEICs. MESFET ICs continue to be developed very energetically. Similarly, GaAs HBT tech-

nology is relatively mature. GaAs quantum well lasers have been shown to be extremely efficient and to have high quantum efficiency and MSM photodetectors have been shown to have high sensitivity and low capacitance. It is expected that GaAs OEICs will play a significant role in local area networks (LAN), for CATV, interoffice systems, and for communication and data links (optical interconnects) in superfast computers.

On the other hand, InP based OEICs are very well matched to optical fiber application and communication systems. Much progress has been made in the development of low-threshold InP lasers and high sensitivity detectors. More recently, significant advances have been made in transistor development, including very high frequency HBTs and FETs as well as MSM detectors. Particularly encouraging are recent advances in growth techniques for InP based material by MOCVD and gas source MBE. Significant advances have also been reported in non-lattice matched epitaxy which might allow the separate optimization of electronic and optical devices.

Given the different potential applications it may be reasonable to expect continued development of both GaAs and InP OEIC technologies.

Conclusions

Over the past several years there has emerged a new area of optoelectronics which integrates photonic and electronic devices. There is now a relative abundance of high quality laser and photodetector structures, made both of GaAs and InP. Transistor structures, FETs and HBTs, suitable for integration with optical devices have also been demonstrated. The rapid development of discrete components has resulted in a number of research prototypes of Optoelectronic Integrated Circuits (OEICs). The most complex circuits demonstrated thus far have been fabricated using GaAs based alloys. InP based ICs are at present less advanced. Since these are better matched to the needs of longer distance fiber communications much effort is devoted to them. While these preliminary OEICs have been difficult to demonstrate it appears now quite feasible to realize high performance generic OEIC chips to meet a number of specific system applications. These include fiber communications and optical switching, board-to-board and computer interconnections, phased array radar signal processing, and many others. OEICs represent an application which can sustain research (universities and industry) while enhancing and advancing today's system capabilities. Because there seem to be applications developing which have performance and part volume requirements commensurate with an integrated technology, it is timely to push development forward.

The key problem in realizing OEICs is the complex interaction of materials growth, processing and device design. In the past, advances in material deposition techniques have been directed mostly towards improving perfection of planar epitaxial layers. In order to satisfy the emerging needs of OEICs more attention will have to be devoted to the growth on patterned surfaces, regrowth on previously processed surfaces etc. Similar advances will have to occur in fabrication procedures designed to avoid damage to the material and thus allow for subsequent overgrowth, fine line lithography on non-planar surfaces and surface passivation. In-situ processing and characterization is at the leading edge of this material growth/processing interaction. The device design and simulation issues appear to be focusing around two generic device pairs: lasers and HBTs, and FETs with p-i-n or MSM detectors. Discrete devices comprising such pairs share many material growth and

fabrication requirements.

Today we find ourselves in a situation of having initial high performance integrated circuits working (GaAs-OEICs) and a range of unique integrated devices under development (InP-PICs). Yet much continued effort is required if these research results are to find applications in systems. It would appear that the time is ripe to begin the task of inserting todays OEICs into real systems while research aimed at improving and extending OEIC capabilities continues in parallel.

The stimulus for further progress will come from "hero" experiments. Some examples are high speed switches being developed for local area networks, integrated coherent receivers [76b], OEIC connector chips, on-chip optical interconnections, integrated photoreceivers, O/E arrays for optical switching, etc.

While these "hero" experiments are most likely to be realized in industrial research and development laboratories, a very significant role will, and should, be played by universities. The recent history of research on discrete devices amply demonstrates the significance of contributions made by university based researchers. It is hoped that this tradition of industry-university collaboration will be encouraged to expand in the area of OEIC research.

Acknowledgements

The authors are indebted to John Crow (IBM), Osamu Wada (Fujitsu) and Martin Pollack (AT&T) for a critical reading of the manuscript and for making numerous suggestions. They are also grateful to the participants to the Hilton Head Workshop for supplying many of the figures used in this report.

Figure Captions

Figure 1. Wavelength Division Multiplex (WDM) system.

Figure 2. Proposed Si/GaAs optical interconnect.

Figure 3. Distributed computer network.

Figure 4. OEIC functions.

Figure 5. Optical neural network.

Figure 6. Phased array antenna system.

Figure 7. Diagram showing the variation of lattice parameter with band-gap energy, as the composition of the III-V ternary compounds is varied. The dotted lines indicate composition ranges which gives rise to indirect band-gap material [after P.K. Tien, unpublished].

Figure 8. Schematic diagram of a laser driver combining InGaAsP laser and a GaAs MESFET.

Figure 9. In-plane hole effective mass dependence on In composition (strain) for $In_xGa_{1-x}As$.

Figure 10. Cathodoluminescence intensity plotted as a function of the etch depth and dot size. Scaling indicates normal surface recombination velocity down to the smallest size.

Figure 11. Schematic diagram of an in-situ processing apparatus consisting of a GSMBE, Ga beam writing, and a dry etching chambers.

Figure 12. Lateral bipolar heterojunction transistor formed by quantum well disordering.

Figure 13. Velocity-field characteristics for different semiconductors.

Figure 14. Tree structure for FETs and bipolar transistors currently being investigated for various electronic applications.

Figure 15. Generic forms of HBTs and FETs and their advantages.

Figure 16. Structures of III-V a)HBTs and b)HEMTs made of different material systems.

Figure 17. Dependence of cut-off frequency on gate length for state-of-the-art FETs.

Figure 18. Tunable InGaAs/InP DBR laser.

Figure 19. GaAs MSM/FET OEIC.

Figure 20. Integration of a photodetector with a waveguide.

Figure 21. Required network interface functions.

Figure 22. Illustration of a space-domain multi-channel task: the optoelectronic cellular array chip.

Figure 23. Different approaches to integrated structures for OEICs.

Figure 24. OEIC transmitter fabricated by a self-aligned planar process [after Toshiba, ref.94].

Figure 25. Plot of demonstrated OEIC vs hybrid receiver performance [after Wada, Fujitsu, ref. 92].

Figure 26. Proposed planar, both optically and electronically compatible, OEIC based on multiple quantum well structures (MQW)[Ref.93].

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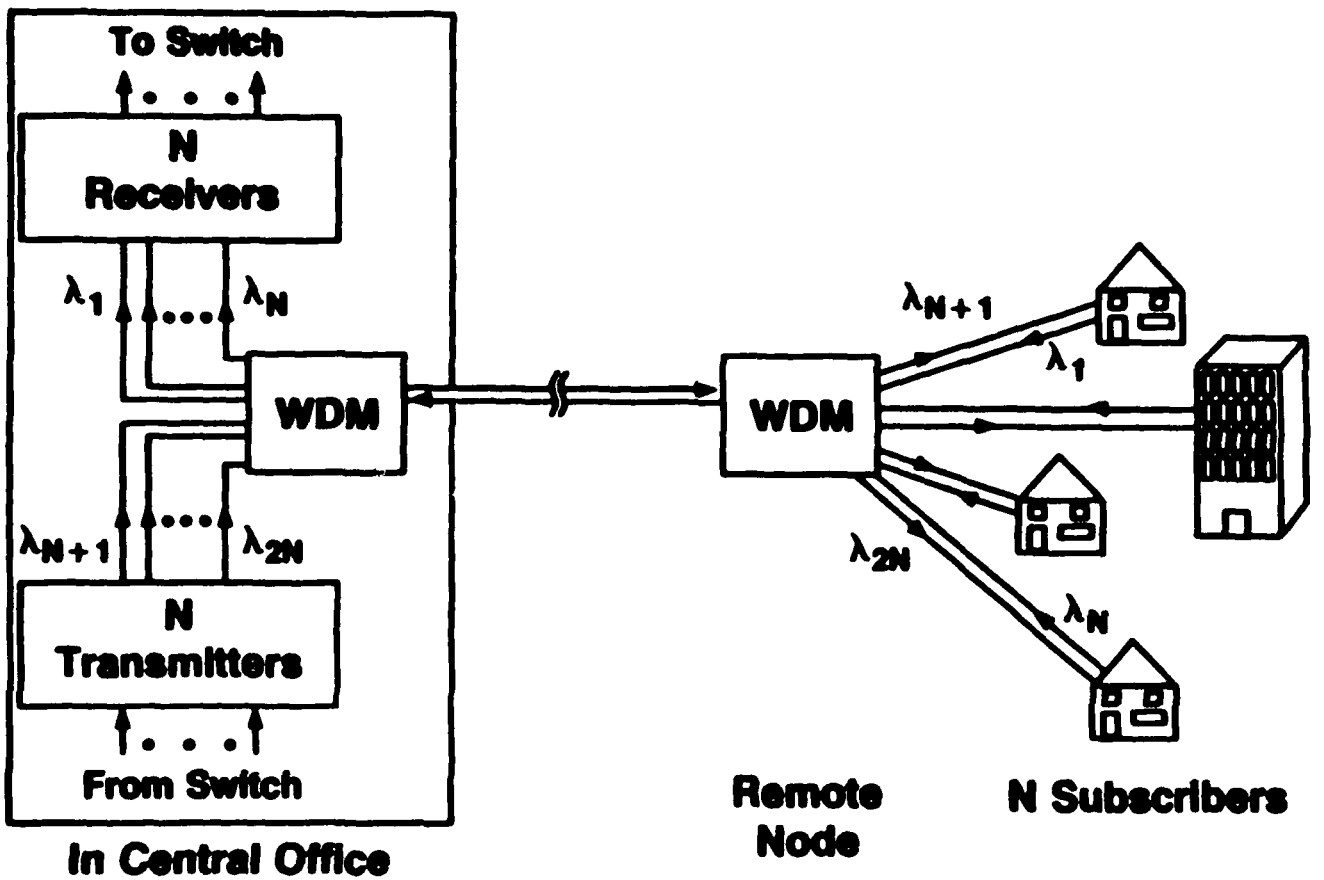

To Switch
N
Receivers
λ_1
λ_N
WDM
λ_{N+1}
λ_{2N}
N
Transmitters
From Switch
In Central Office
WDM
λ_{N+1}
λ_1
λ_{2N}
λ_N
Remote
Node
N Subscribers

Figure 1

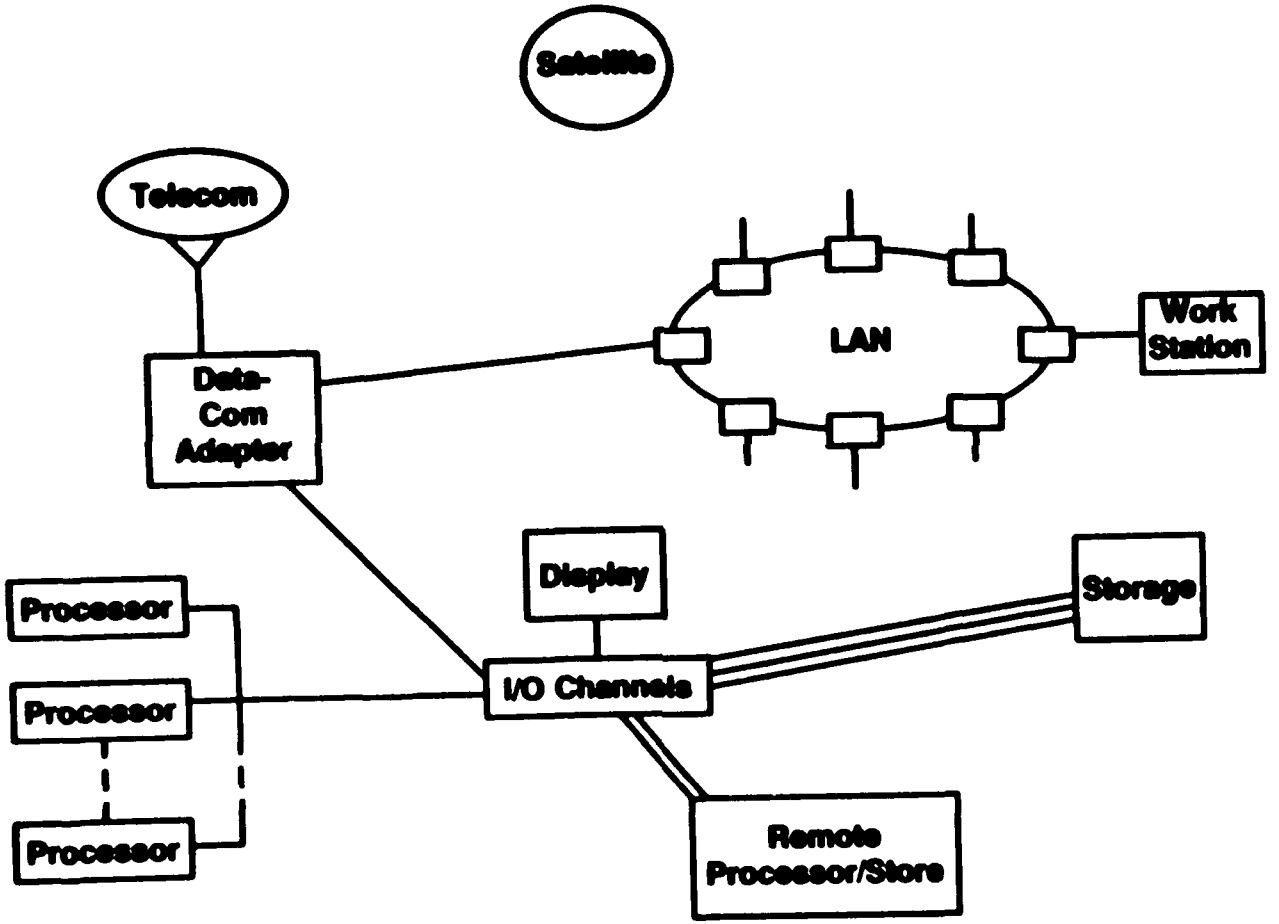

Satellite
Telecom
LAN
Work Station
Data-Com Adapter
Display
Storage
Processor
Processor
Processor
I/O Channels
Remote Processor/Store

FIgure 2

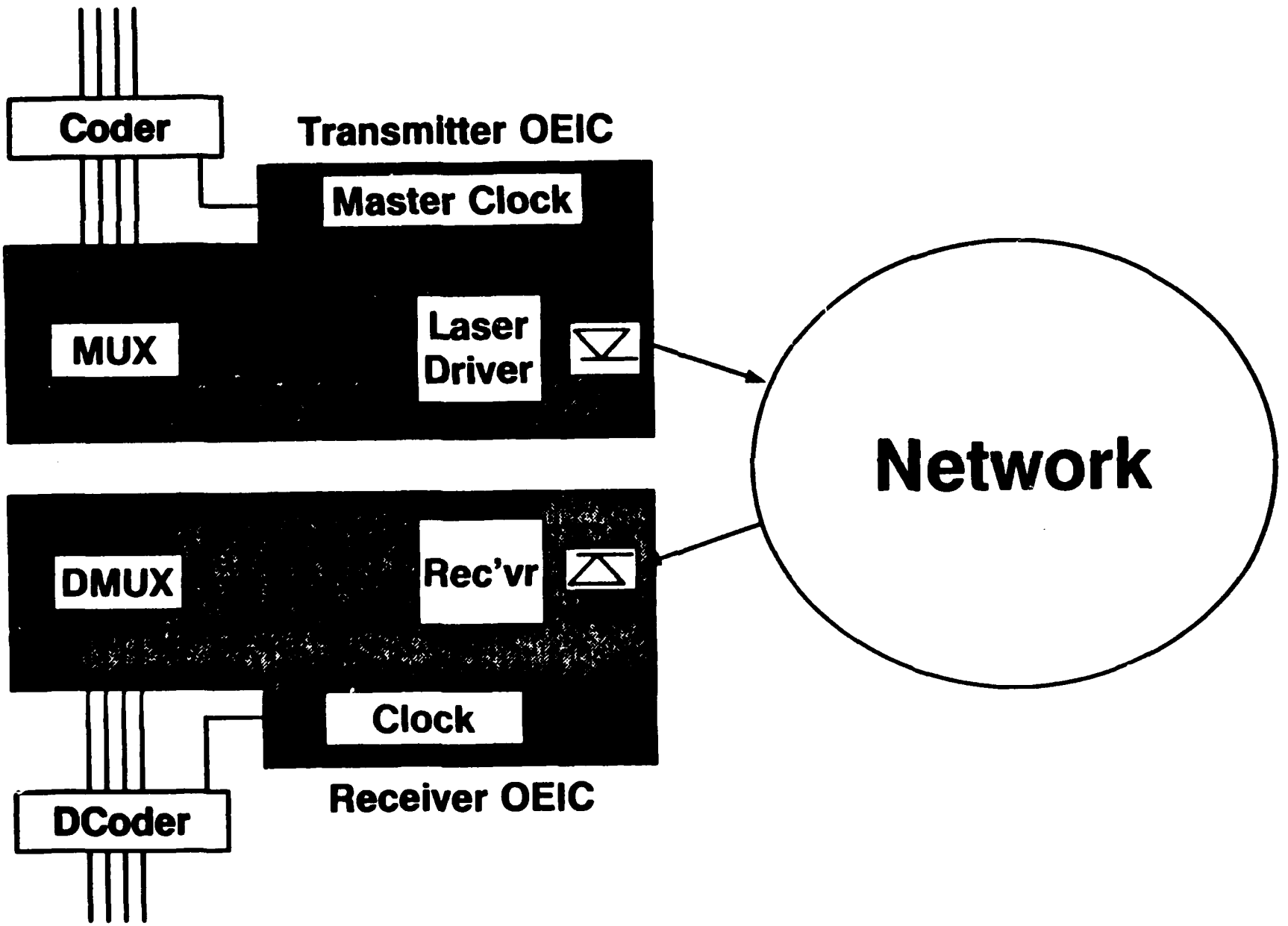

Coder
Transmitter OEIC
Master Clock
MUX
Laser
Driver
Network
DMUX
Rec'vr
Clock
DCoder
Receiver OEIC

Figure 3

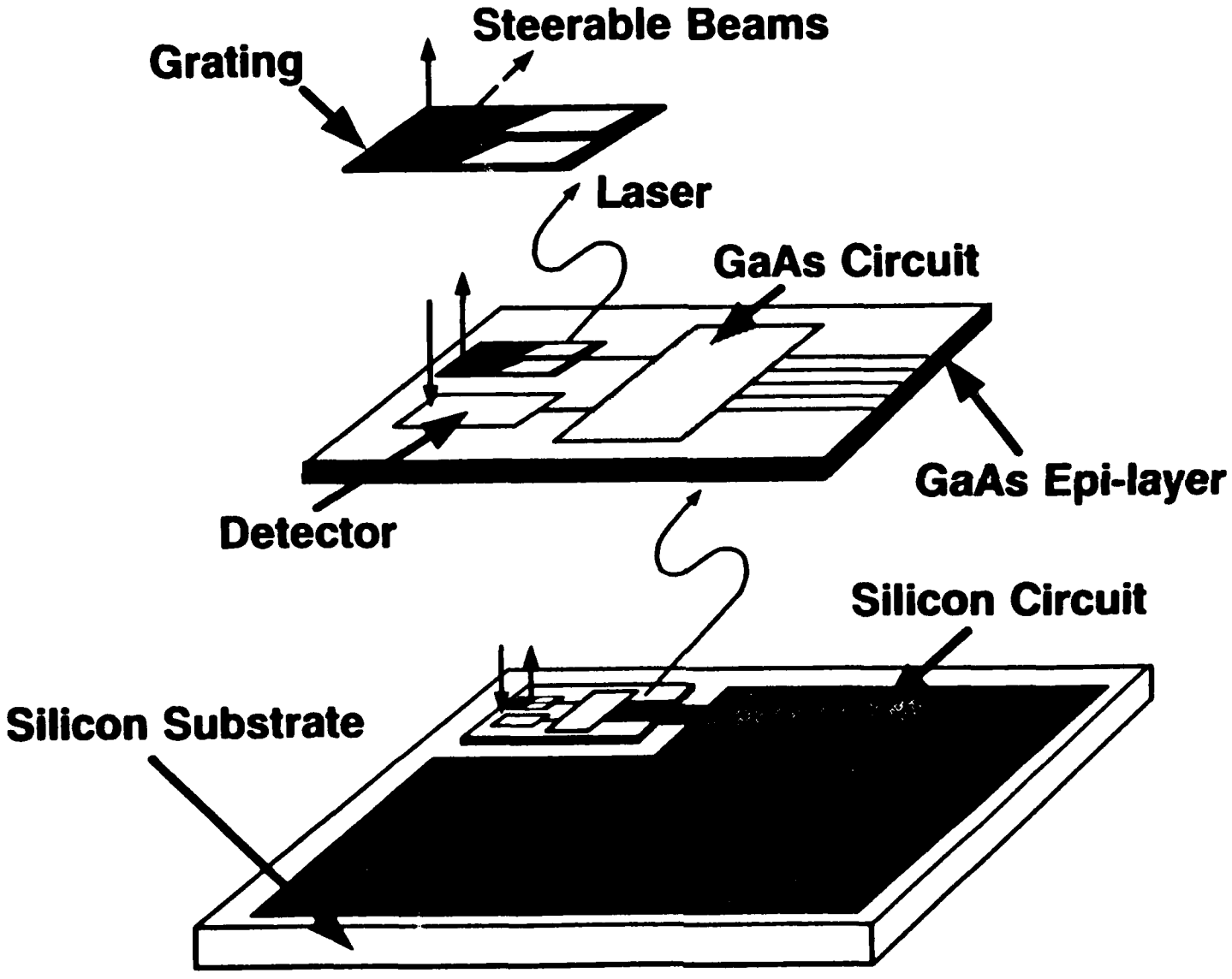

Steerable Beams
Grating
Laser
GaAs Circuit
GaAs Epi-layer
Detector
Silicon Circuit
Silicon Substrate

Figure 4

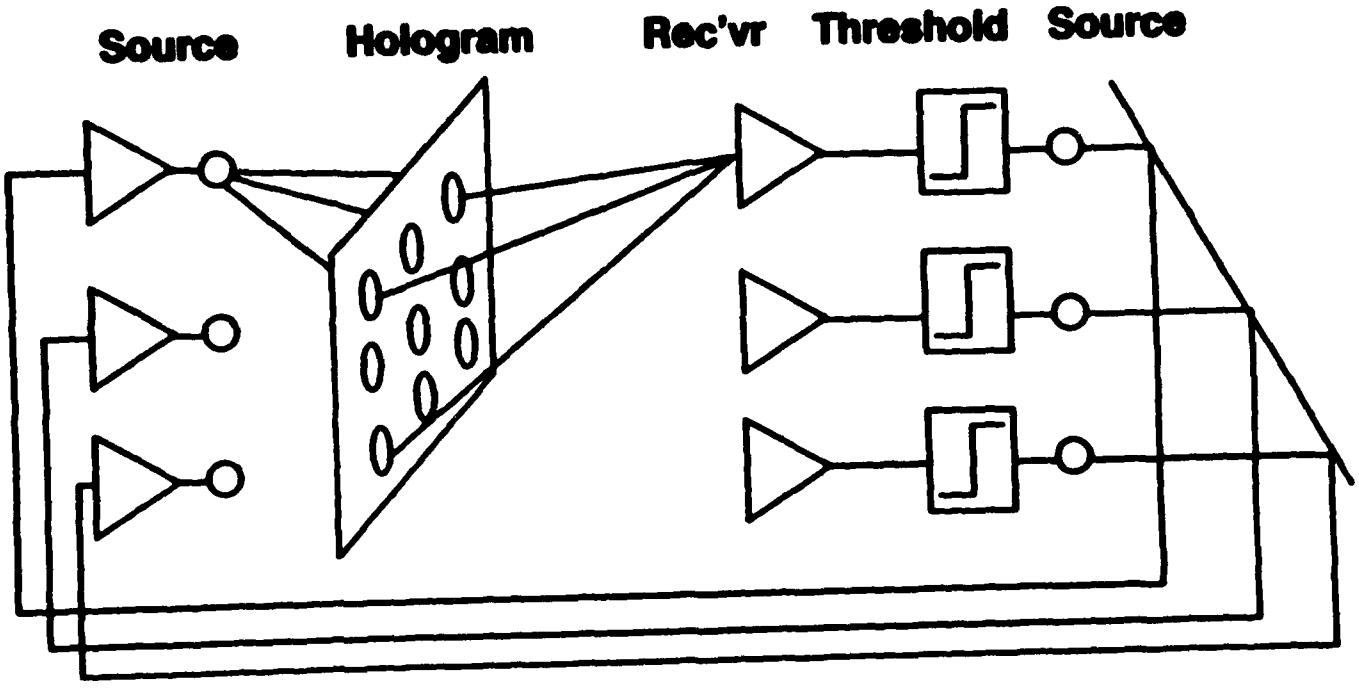


Figure 5

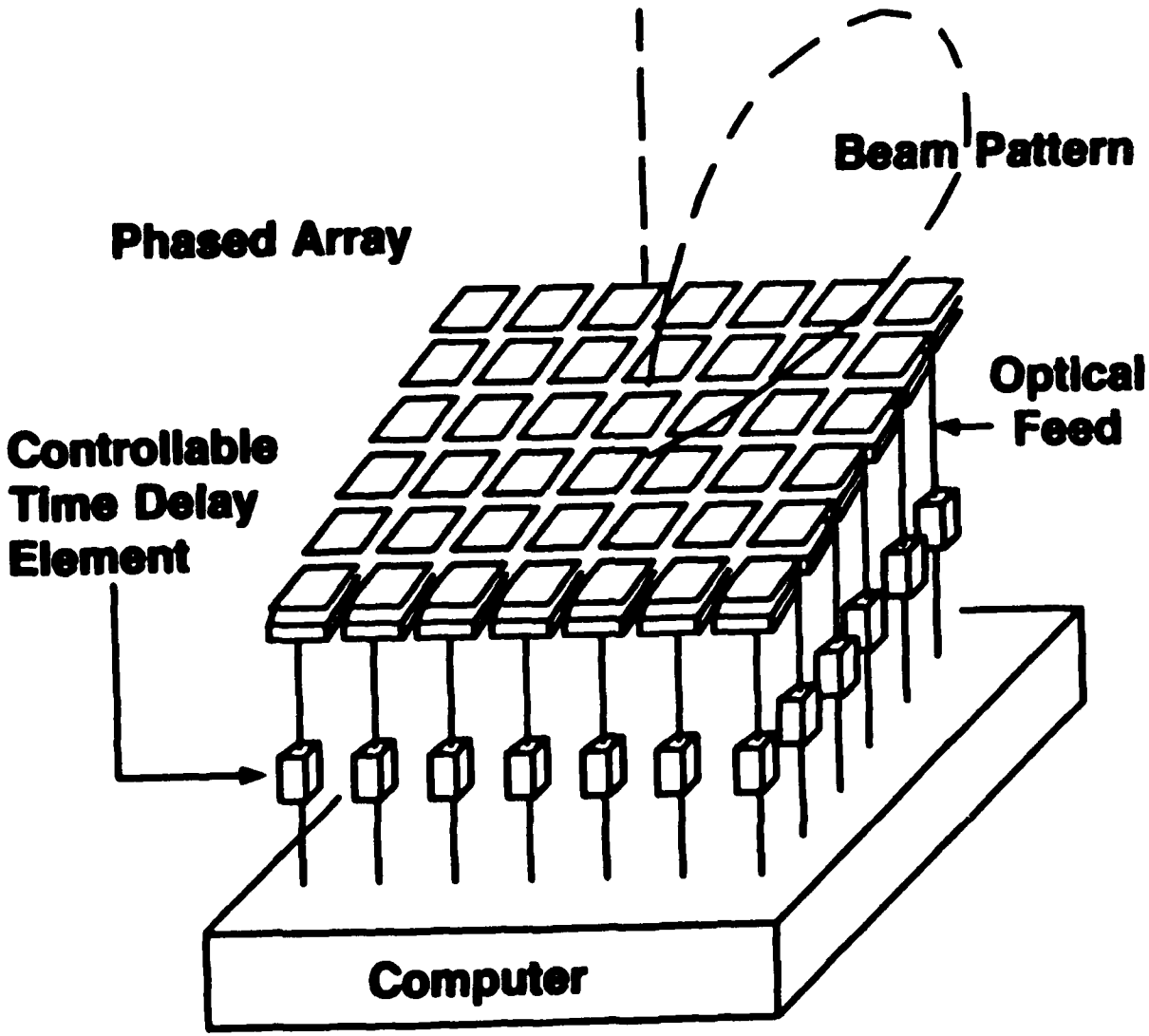

Beam Pattern
Phased Array
Optical
Feed
Controllable
Time Delay
Element
Computer

Figure 6

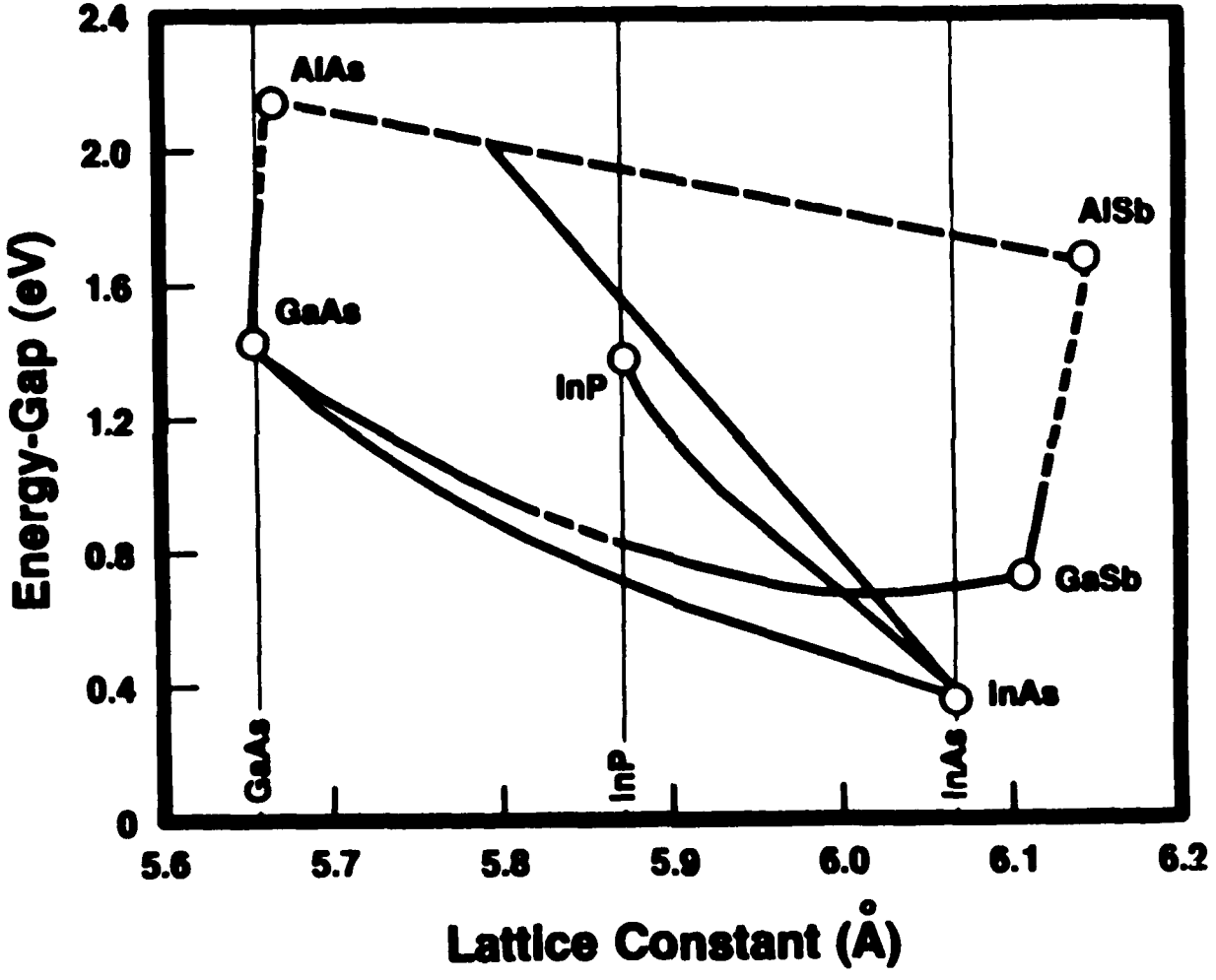

2.4
2.0
1.6
1.2
0.8
0.4
0
Energy-Gap (eV)
AlAs
AlSb
GaAs
InP
GaSb
InAs
GaAs
InP
InAs
5.6
5.7
5.8
5.9
6.0
6.1
6.2
Lattice Constant (Å)

Figure 7

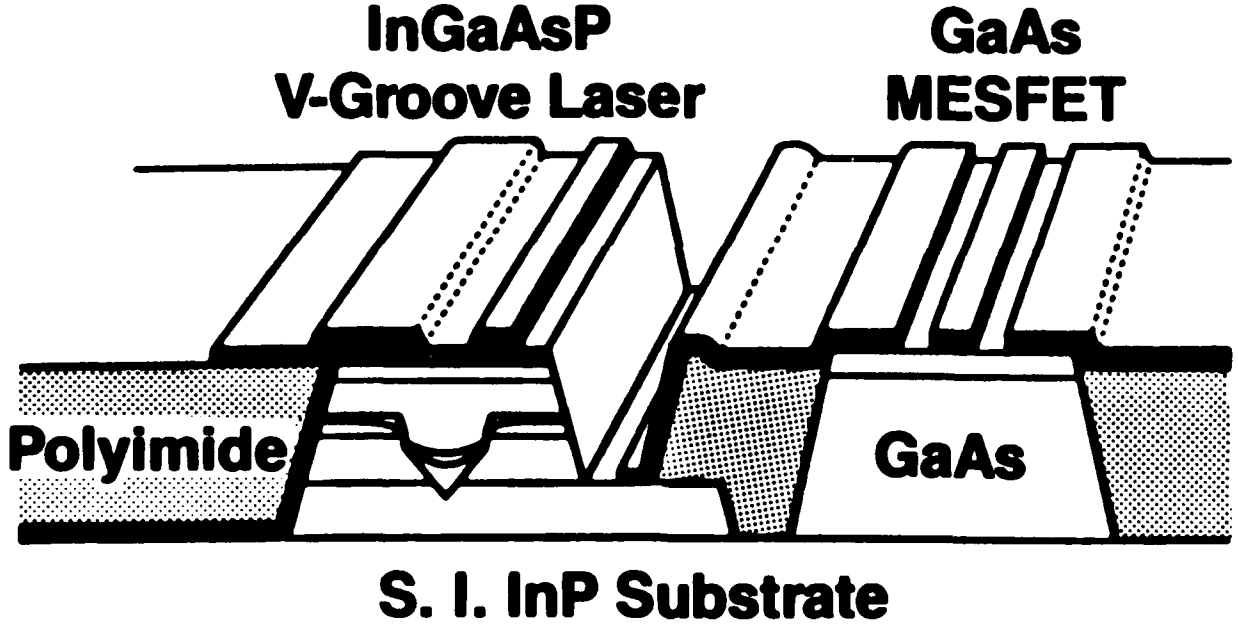

InGaAsP
V-Groove Laser
GaAs
MESFET
Polyimide
GaAs
S. I. InP Substrate

Figure 8

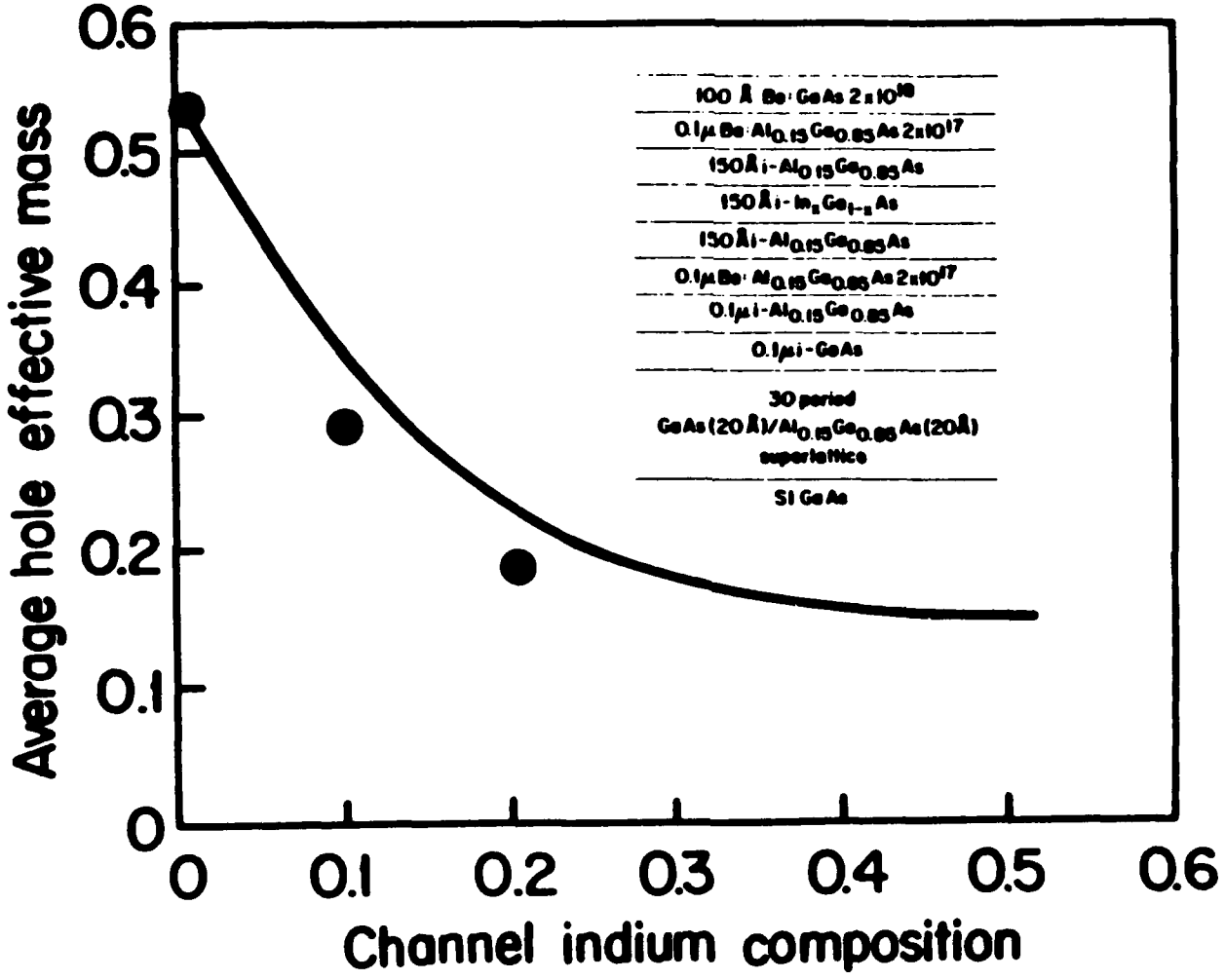

Average hole effective mass
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.1
0.2
0.3
0.4
0.5
0.6
Channel indium composition
100 Å Be·GaAs 2×10^18
0.1μ Be·Al0.15Ga0.85As 2×10^17
150Å i-Al0.15Ga0.85As
150Å i-InxGa1-xAs
150Å i-Al0.15Ga0.85As
0.1μ Be·Al0.15Ga0.85As 2×10^17
0.1μ i-Al0.15Ga0.85As
0.1μ i-GaAs
30 period
GaAs(20Å)/Al0.15Ga0.85As(20Å)
superlattice
SI GaAs

Figure 9

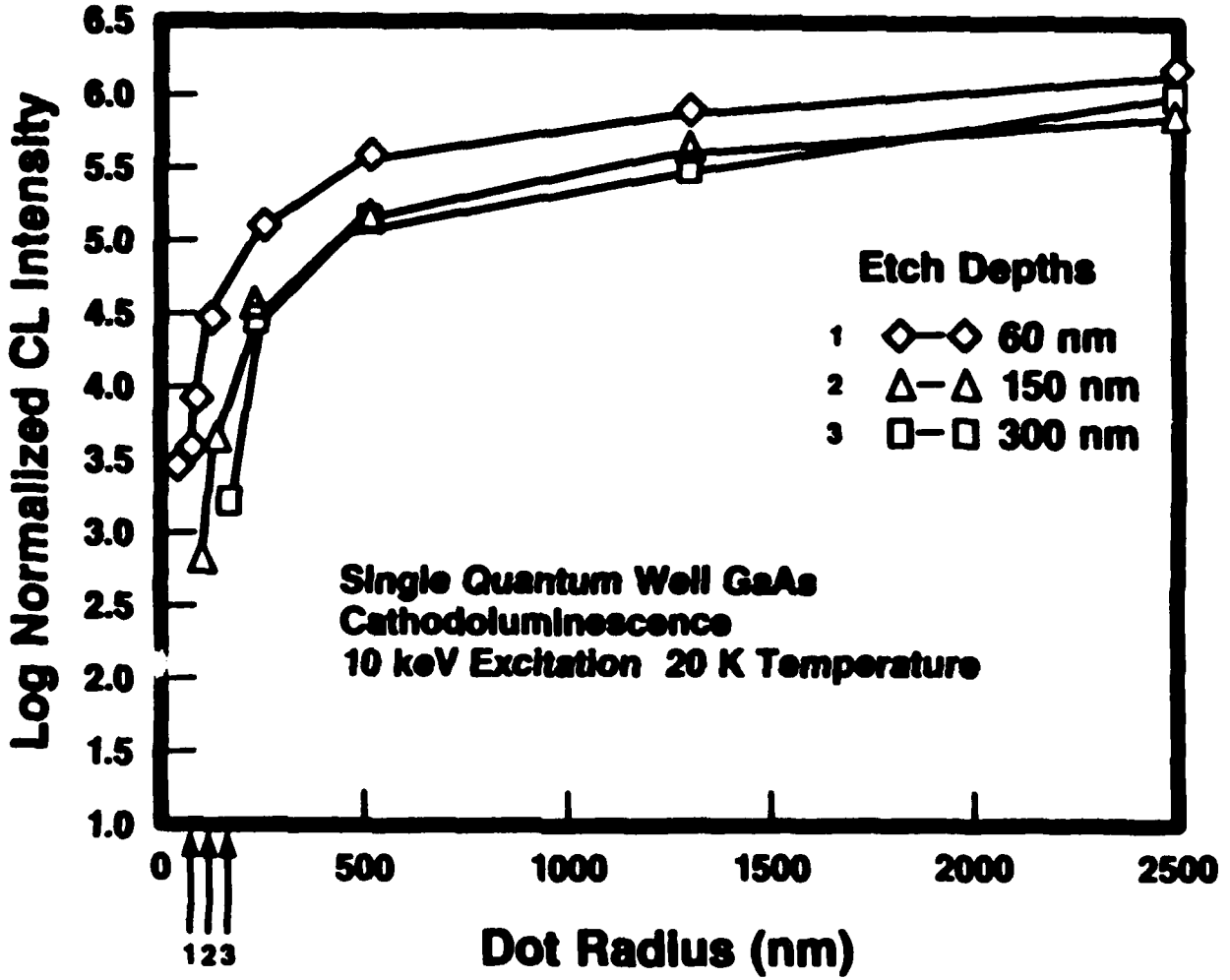

CL Intensity vs Etch Depth and Dot Size
Log Normalized CL Intensity
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0
500
1000
1500
2000
2500
Dot Radius (nm)
1 2 3
Etch Depths
1 60 nm
2 150 nm
3 300 nm
Single Quantum Well GaAs
Cathodoluminescence
10 keV Excitation 20 K Temperature

Figure 10

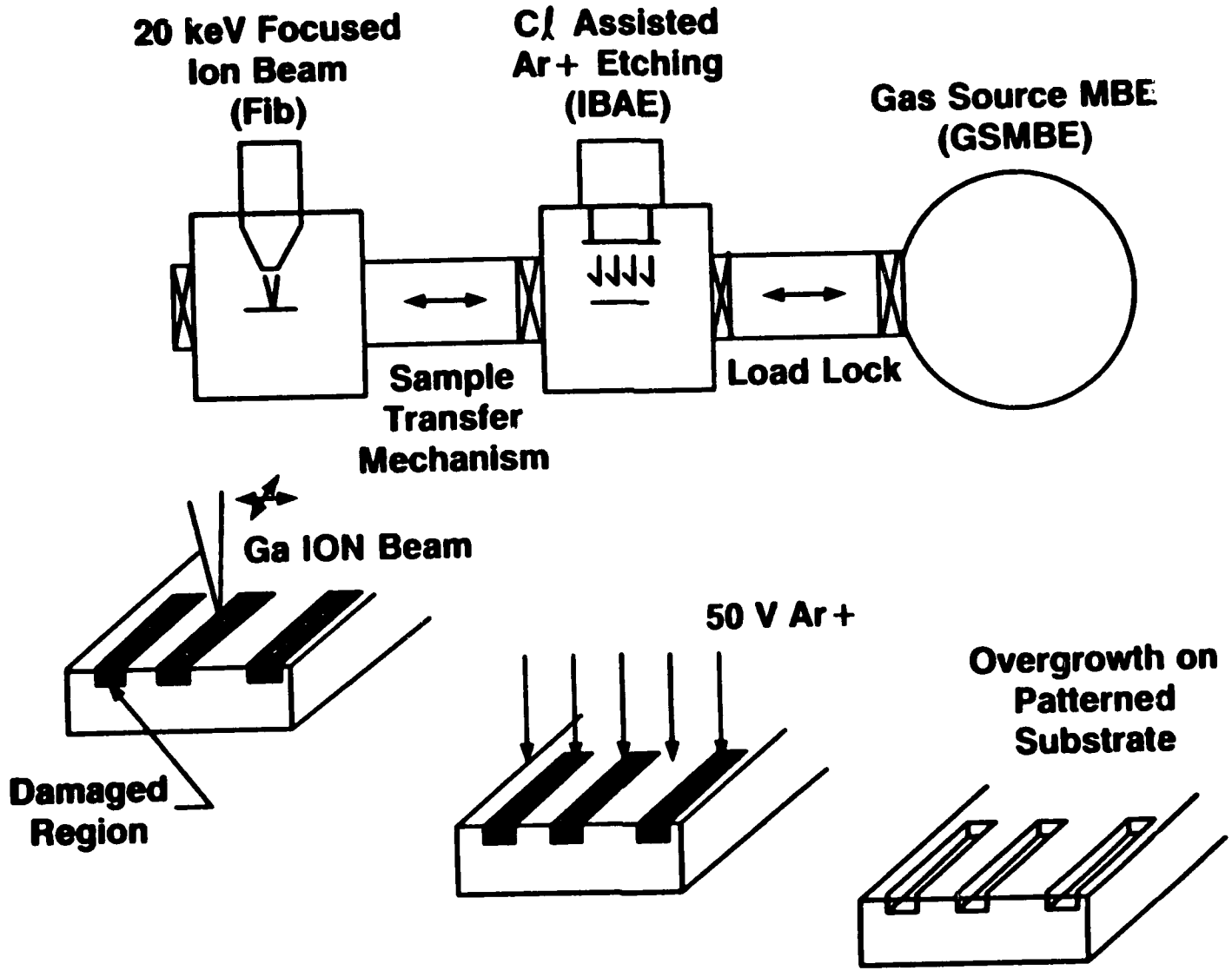

20 keV Focused
Ion Beam
(Fib)
Cl Assisted
Ar+ Etching
(IBAE)
Gas Source MBE
(GSMBE)
Sample
Transfer
Mechanism
Load Lock
Ga ION Beam
Damaged
Region
50 V Ar+
Overgrowth on
Patterned
Substrate

Figure 11

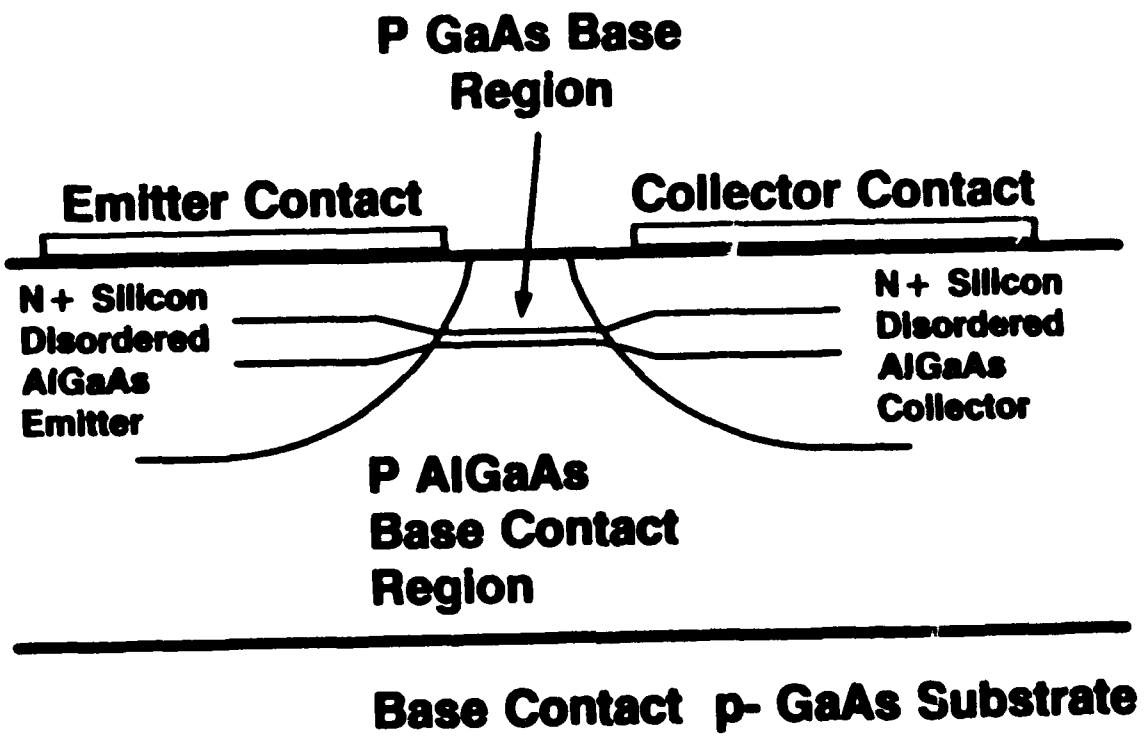

P GaAs Base
Region
Emitter Contact
Collector Contact
N+ Silicon
Disordered
AlGaAs
Emitter
N+ Silicon
Disordered
AlGaAs
Collector
P AlGaAs
Base Contact
Region
Base Contact p- GaAs Substrate

Figure 12

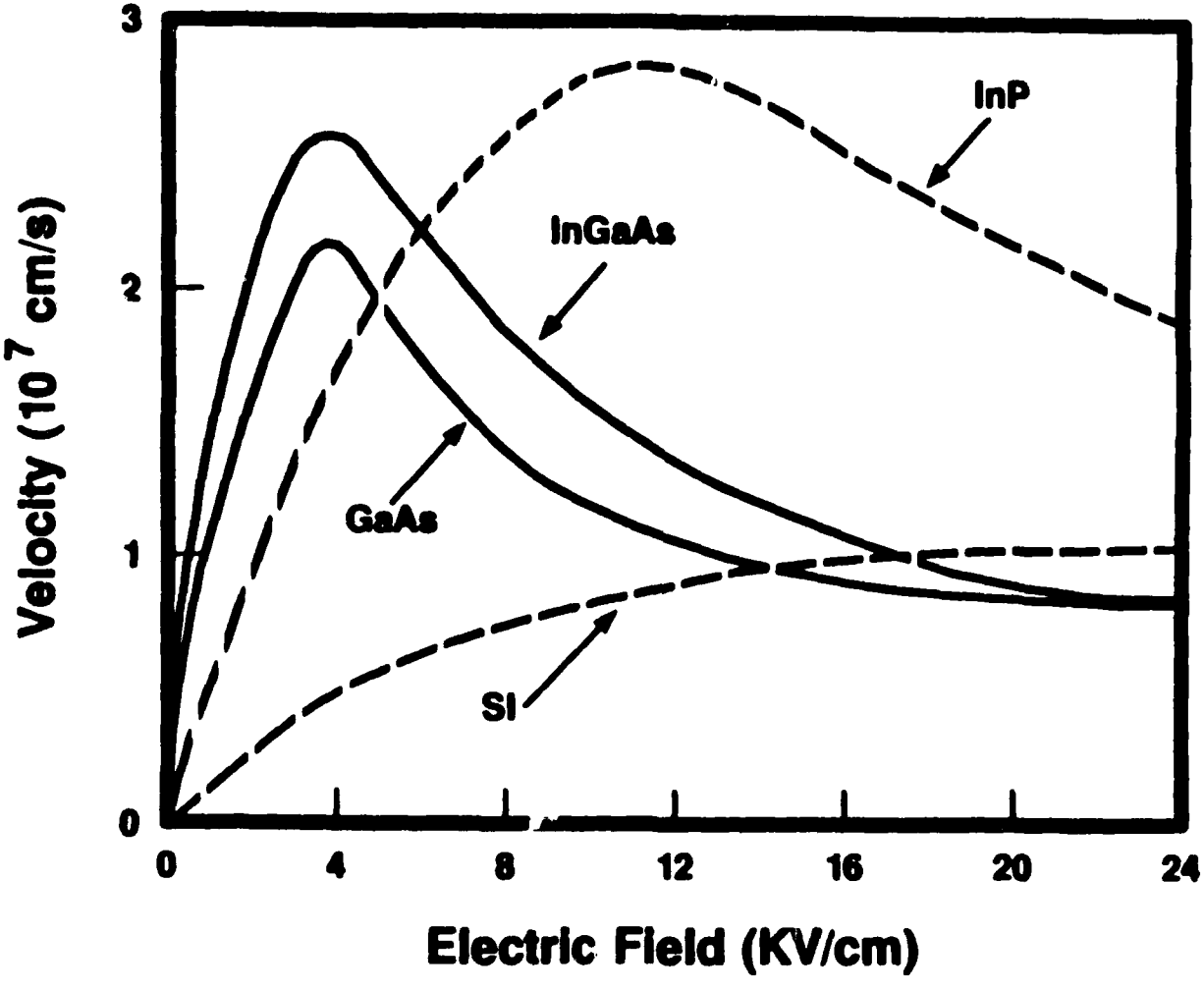

Velocity (10^7 cm/s)
3
2
1
0
0
4
8
12
16
20
24
Electric Field (KV/cm)
InP
InGaAs
GaAs
SI

Figure 13

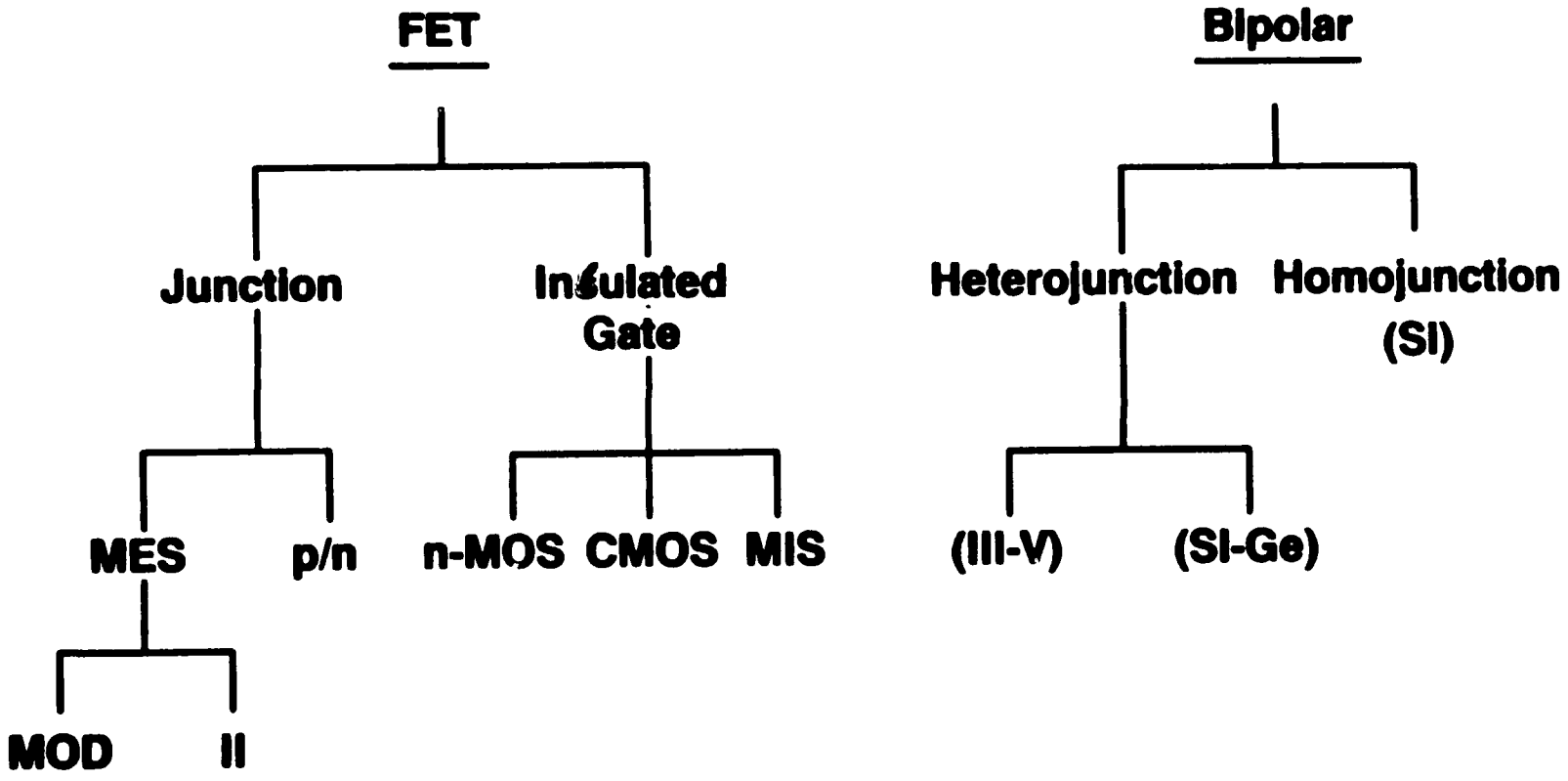
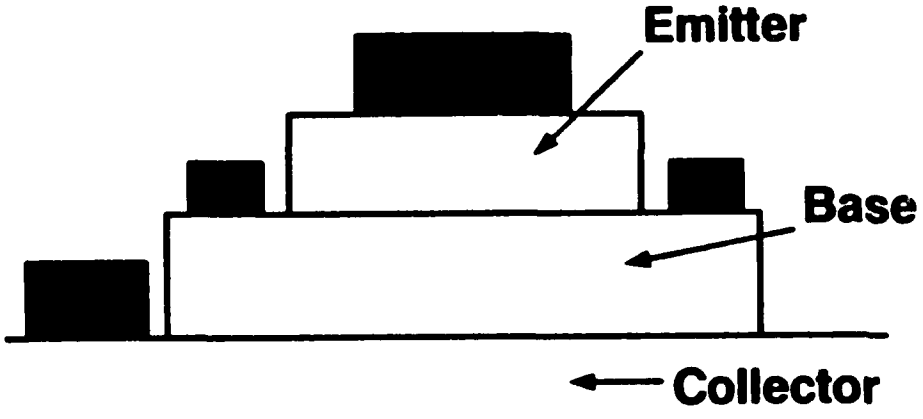
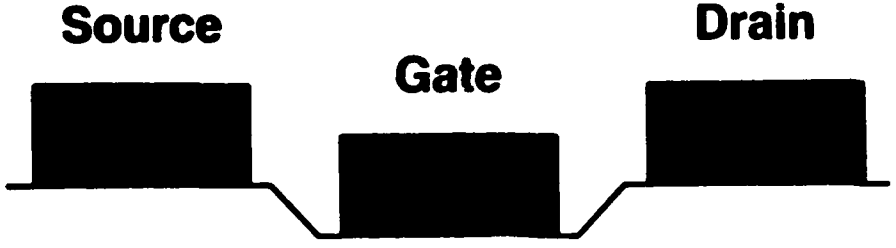

FET
Junction
Insulated Gate
MES
p/n
n-MOS
CMOS
MIS
MOD
II
Bipolar
Heterojunction
Homojunction (SI)
(III-V)
(SI-Ge)

Figure 14



HBT Advantages

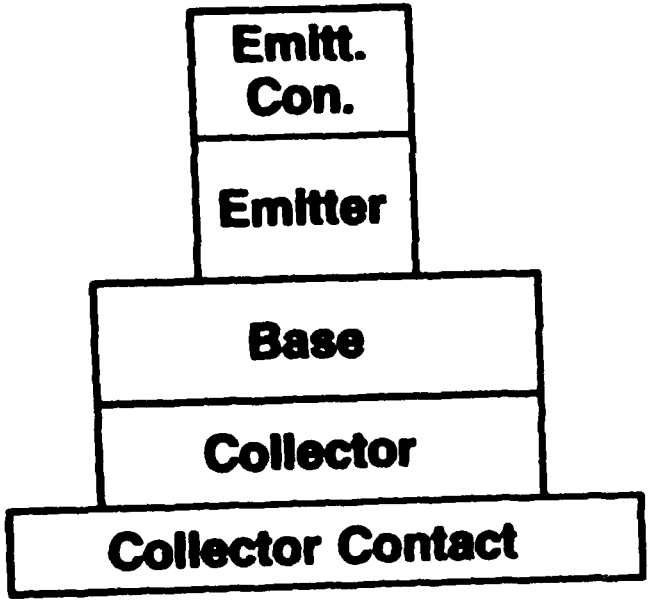
- Vertical Device
  - High density
  - Critical dimensions
- High Current Drive
  - Insensitive to fan-out
- High Transconductance
  - Low voltage swings
- Uniform Threshold
  - Determined by band gap



FET Advantages

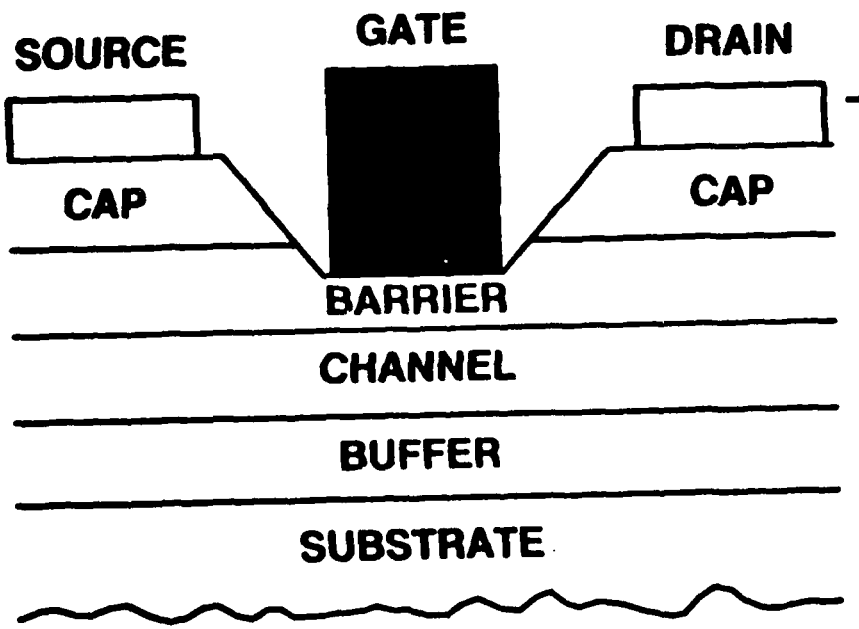
- High Input Inpedance
- Low Parasitic Capacitances
- No Stored Charge in Saturation

Figure 15



	AlGaAs HBT	InP HBT	AlInAs HBT
Emitt. Con.	n GaAs	n InGaAs	n InGaAs
Emitter	n AlGaAs	n InP	n AlInAs
Base	p GaAs	p InGaAs	p InGaAs
Collector	n GaAs	n InGaAs	n InGaAs
Collector Contact	n GaAs	n InGaAs	n InGaAs

Figure 16a



	AlGaAs HEMT	InGaAs Pseudomorphic HEMT	InGaAs HEMT
CAP	N+ GaAs	N+ GaAs	N+ $In_{.53}Ga_{.47}As$
BARRIER	N+ $Al_{.3}Ga_{.7}As$	N $Al_{.15}Ga_{.85}As$	N $Al_{.48}In_{.52}As$
CHANNEL	P- GaAs	P- $In_{.15}Ga_{.85}As$	N- $In_{.53}Ga_{.47}As$
BUFFER	P- GaAs	P- GaAs	N- $Al_{.48}In_{.52}As$
SUBSTRATE	SI GaAs	SI GaAs	SI InP

Figure 16b

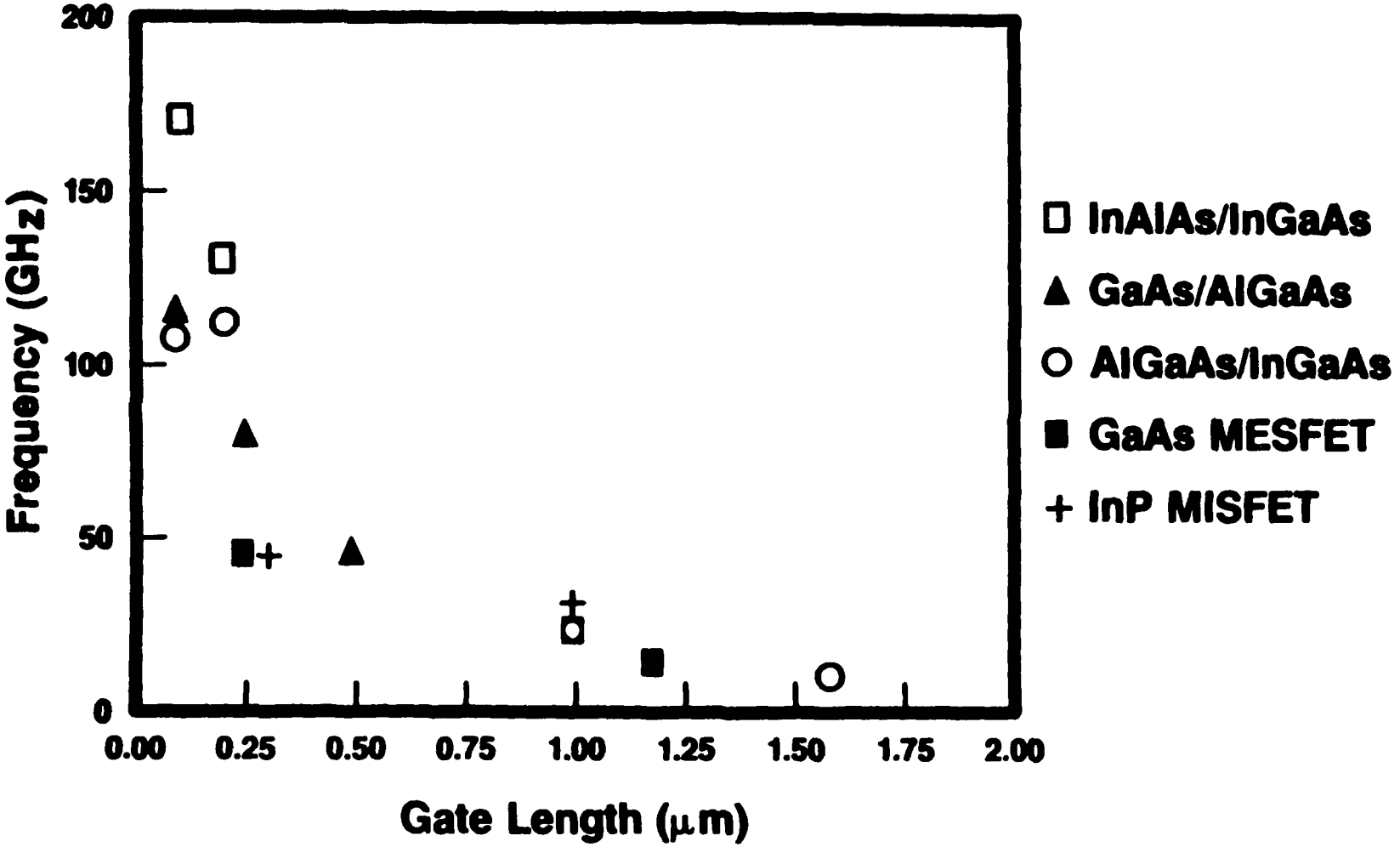

200
150
100
50
0
Frequency (GHz)
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
Gate Length (μm)
InAlAs/InGaAs
GaAs/AlGaAs
AlGaAs/InGaAs
GaAs MESFET
InP MISFET

Figure 17

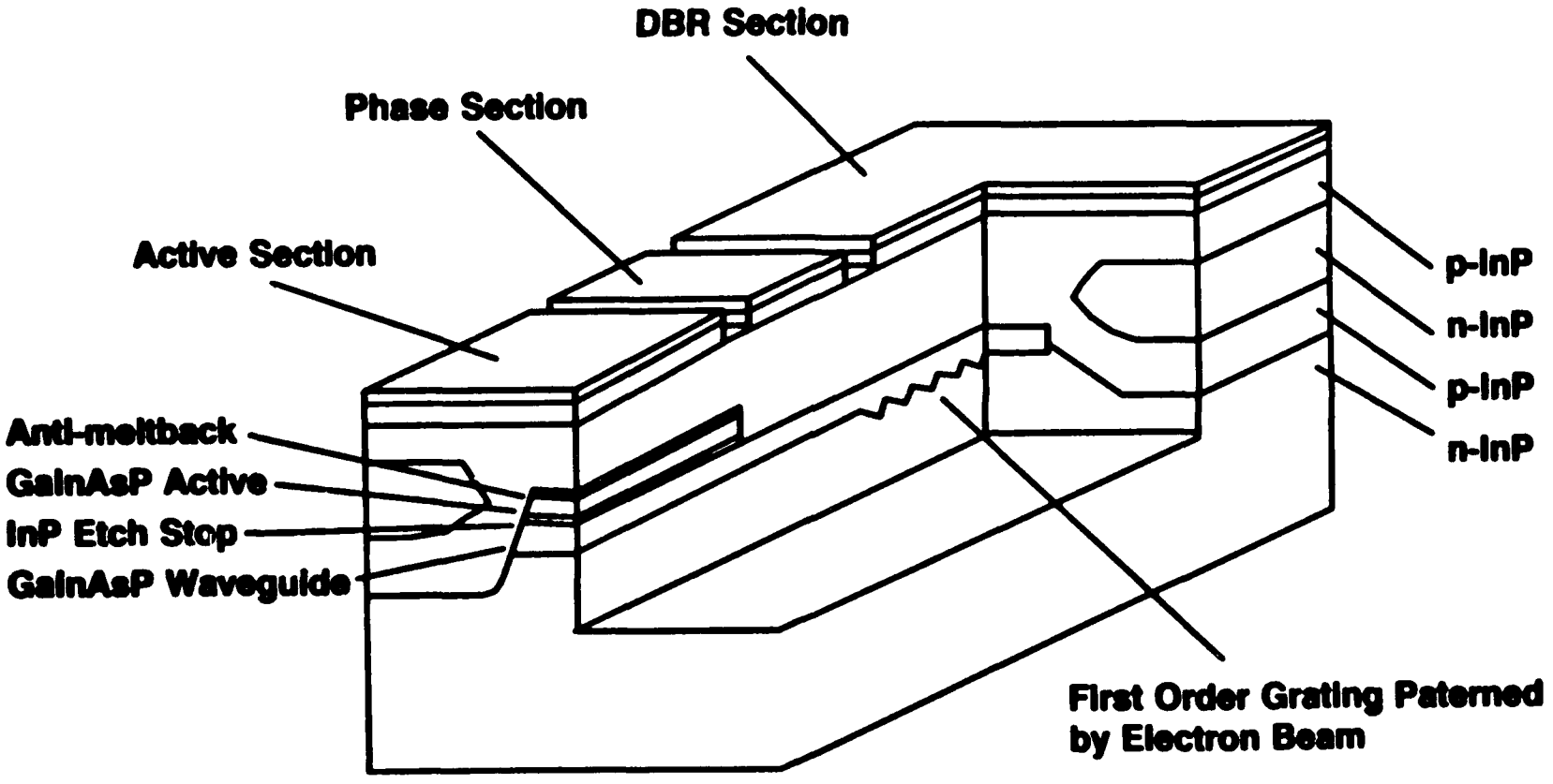

DBR Section
Phase Section
Active Section
Anti-meltback
GaInAsP Active
InP Etch Stop
GaInAsP Waveguide
p-InP
n-InP
p-InP
n-InP
First Order Grating Patterned
by Electron Beam

Figure 18

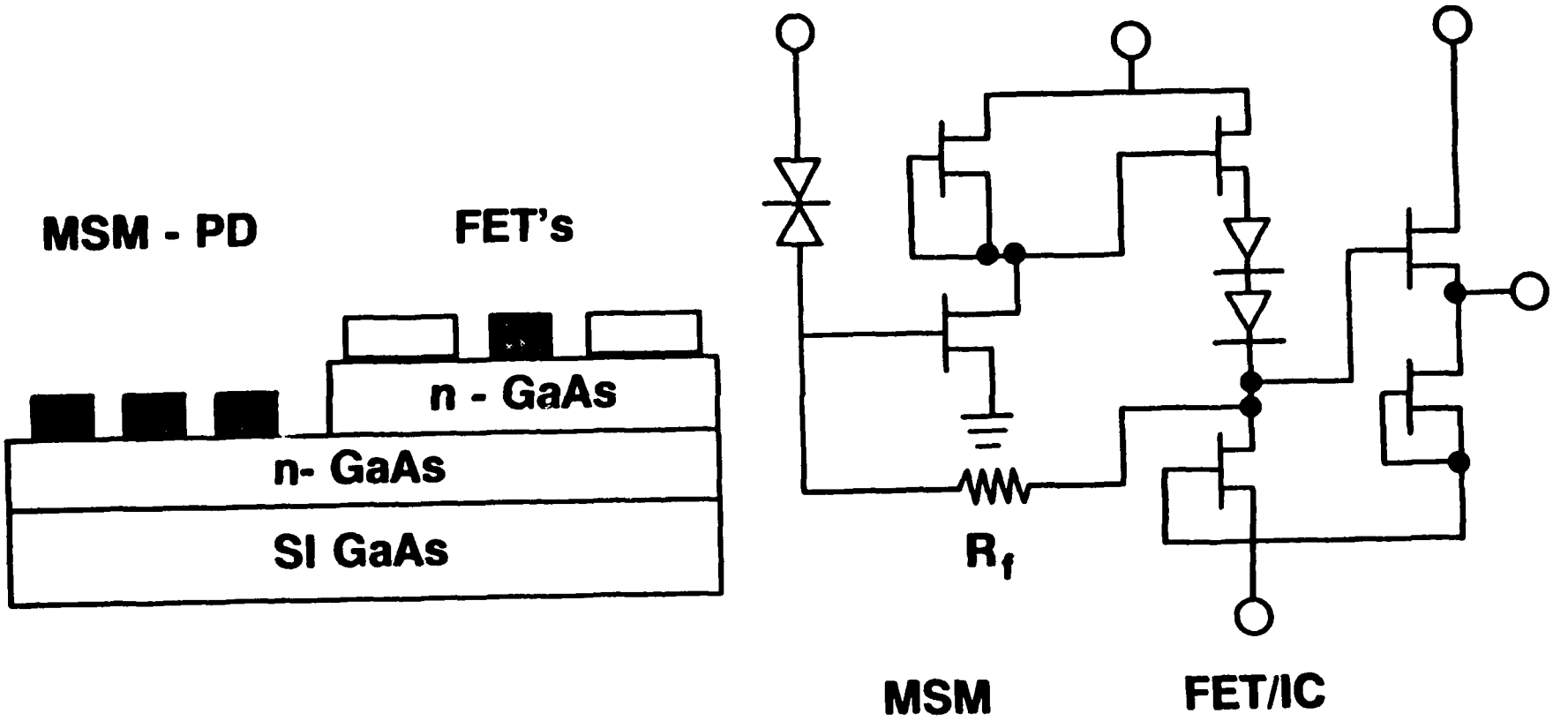


Figure 19

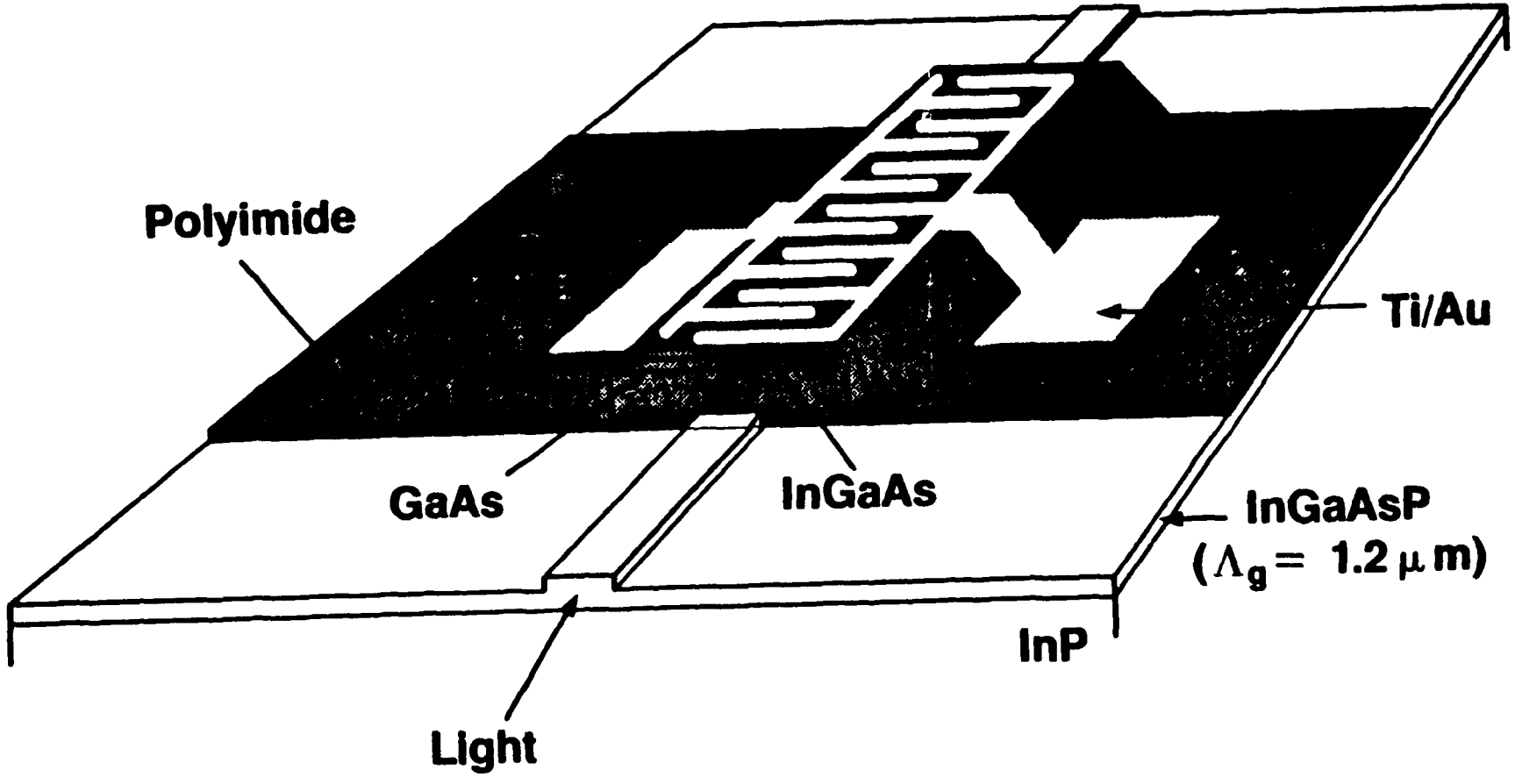


Figure 20

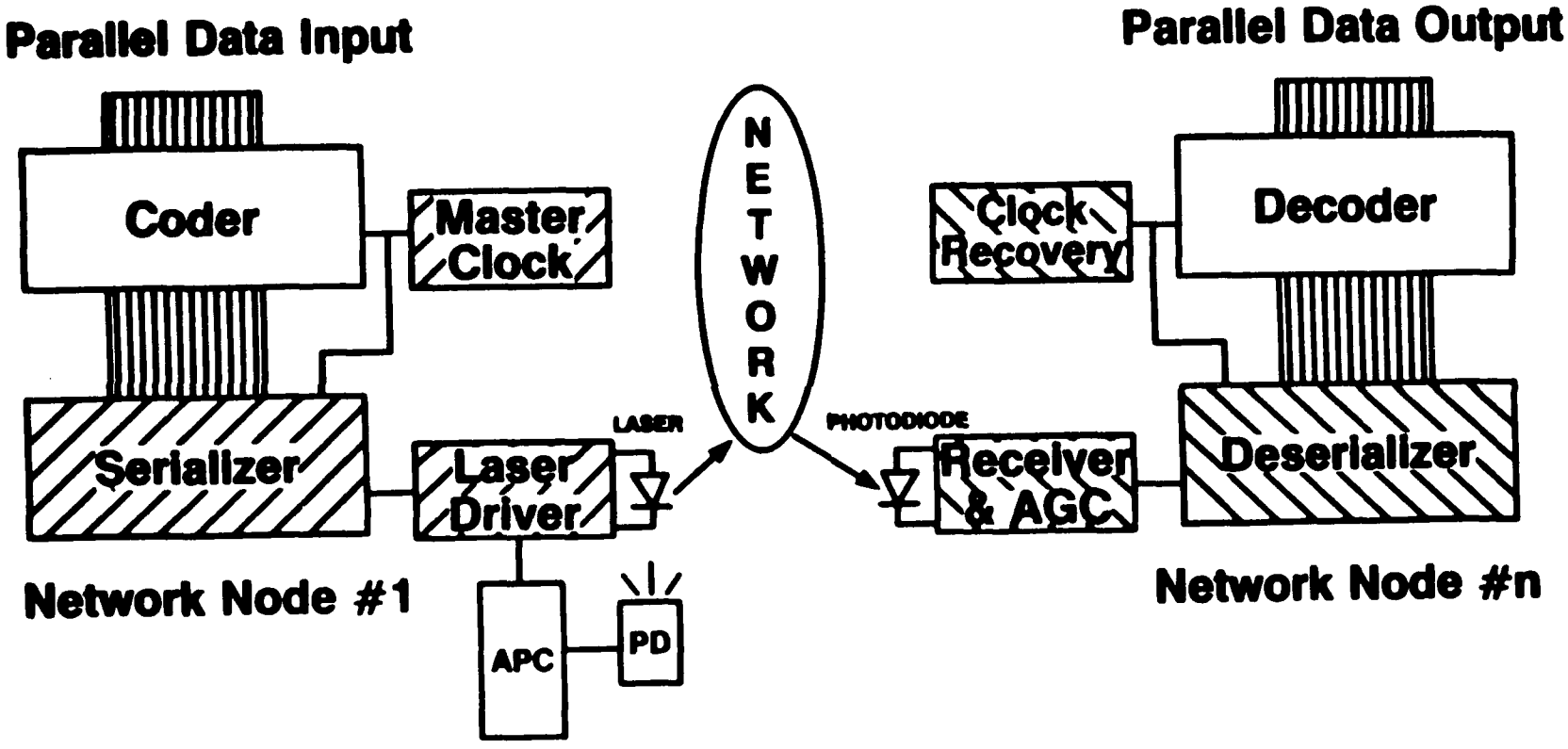

Parallel Data Input
Parallel Data Output
Coder
Master Clock
NETWORK
Clock Recovery
Decoder
Serializer
Laser Driver
LASER
PHOTODIODE
Receiver & AGC
Deserializer
Network Node #1
Network Node #n
APC
PD

Figure 21

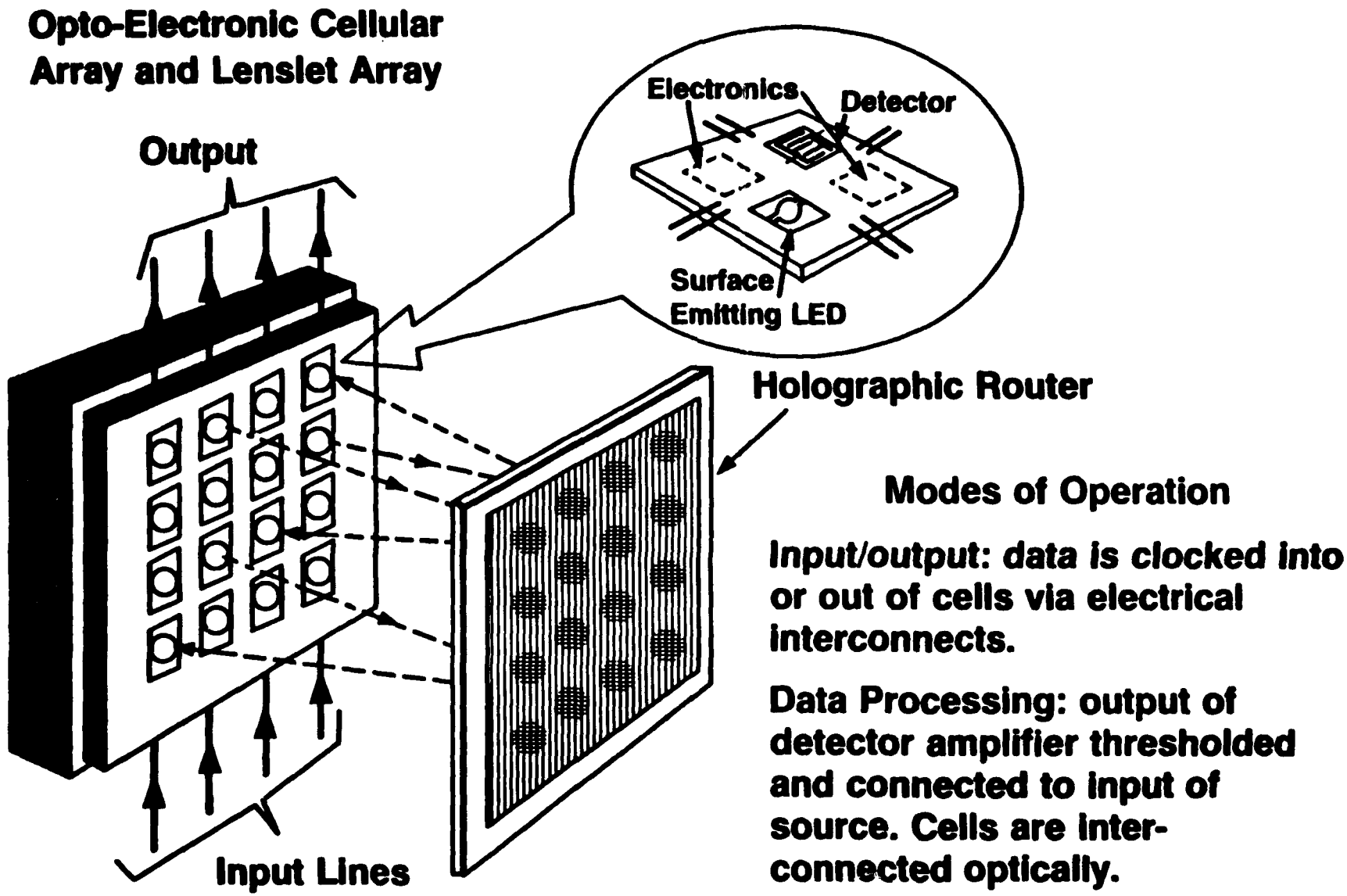

Opto-Electronic Cellular
Array and Lenslet Array
Output
Electronics
Detector
Surface
Emitting LED
Holographic Router
Input Lines
Modes of Operation
Input/output: data is clocked into or out of cells via electrical interconnects.
Data Processing: output of detector amplifier thresholded and connected to input of source. Cells are inter-connected optically.

Figure 22

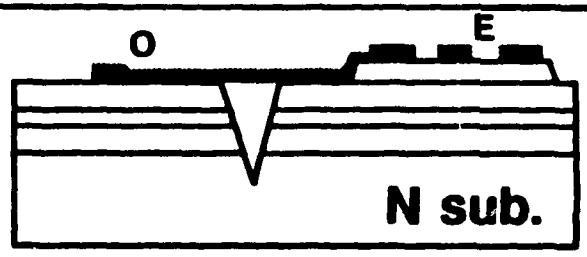
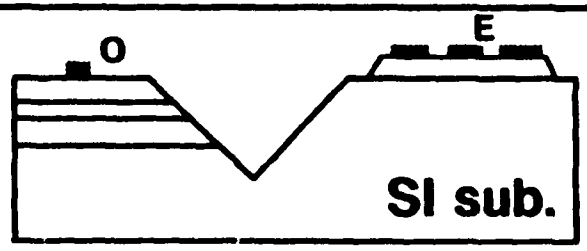
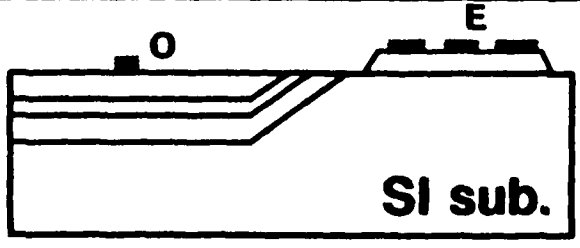
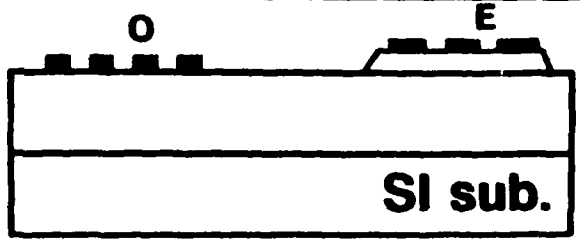
Structure	Cross-section
Vertical	
Graded-step	
Planar-embedded	
Planar, compatible	

Figure 23

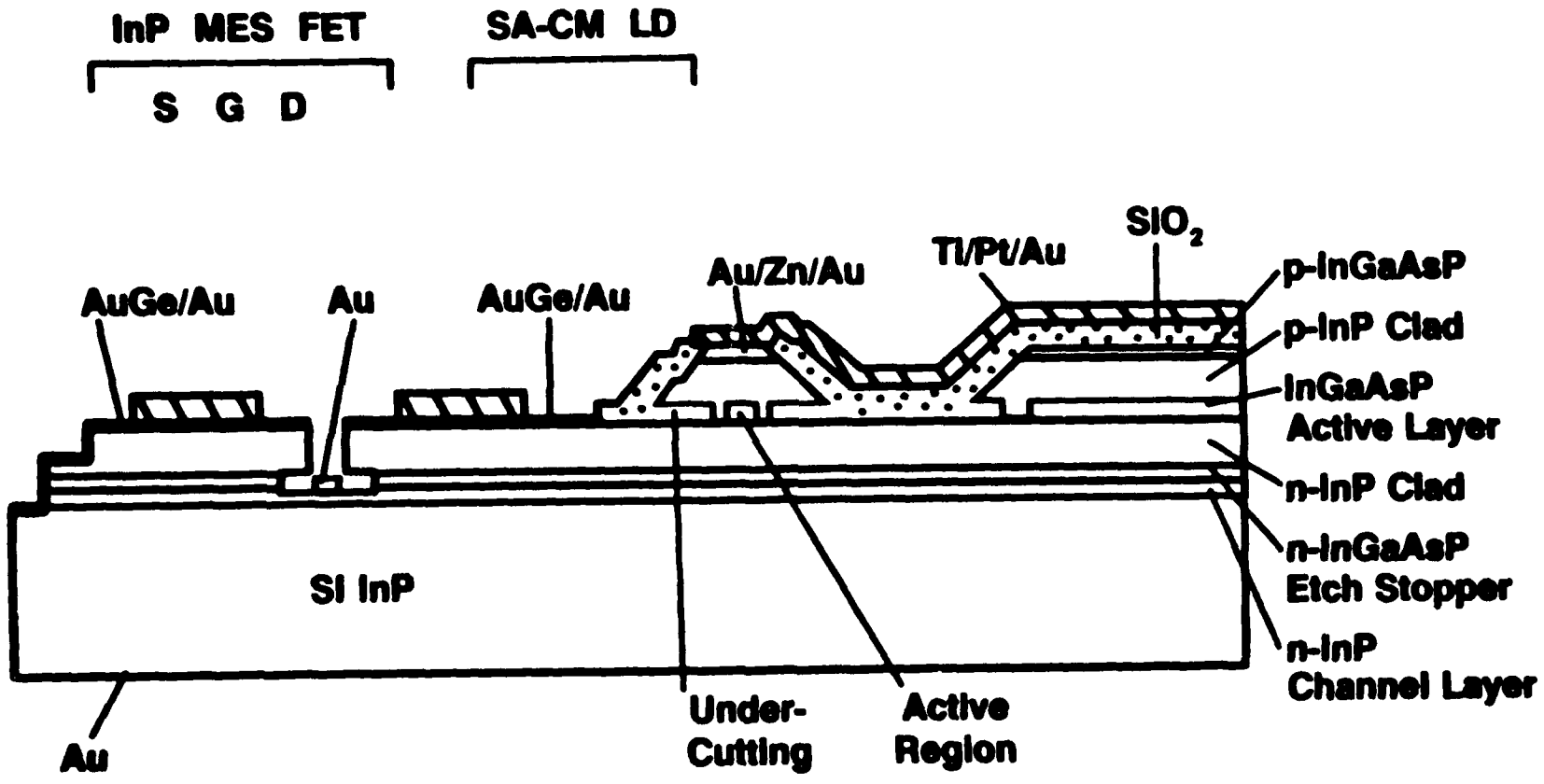

InP MES FET
SA-CM LD
S G D
AuGe/Au
Au
AuGe/Au
Au/Zn/Au
Ti/Pt/Au
SiO2
p-InGaAsP
p-InP Clad
InGaAsP
Active Layer
n-InP Clad
n-InGaAsP
Etch Stopper
n-InP
Channel Layer
SI InP
Au
Under-
Cutting
Active
Region

Figure 24

OEIC Receiver Performance

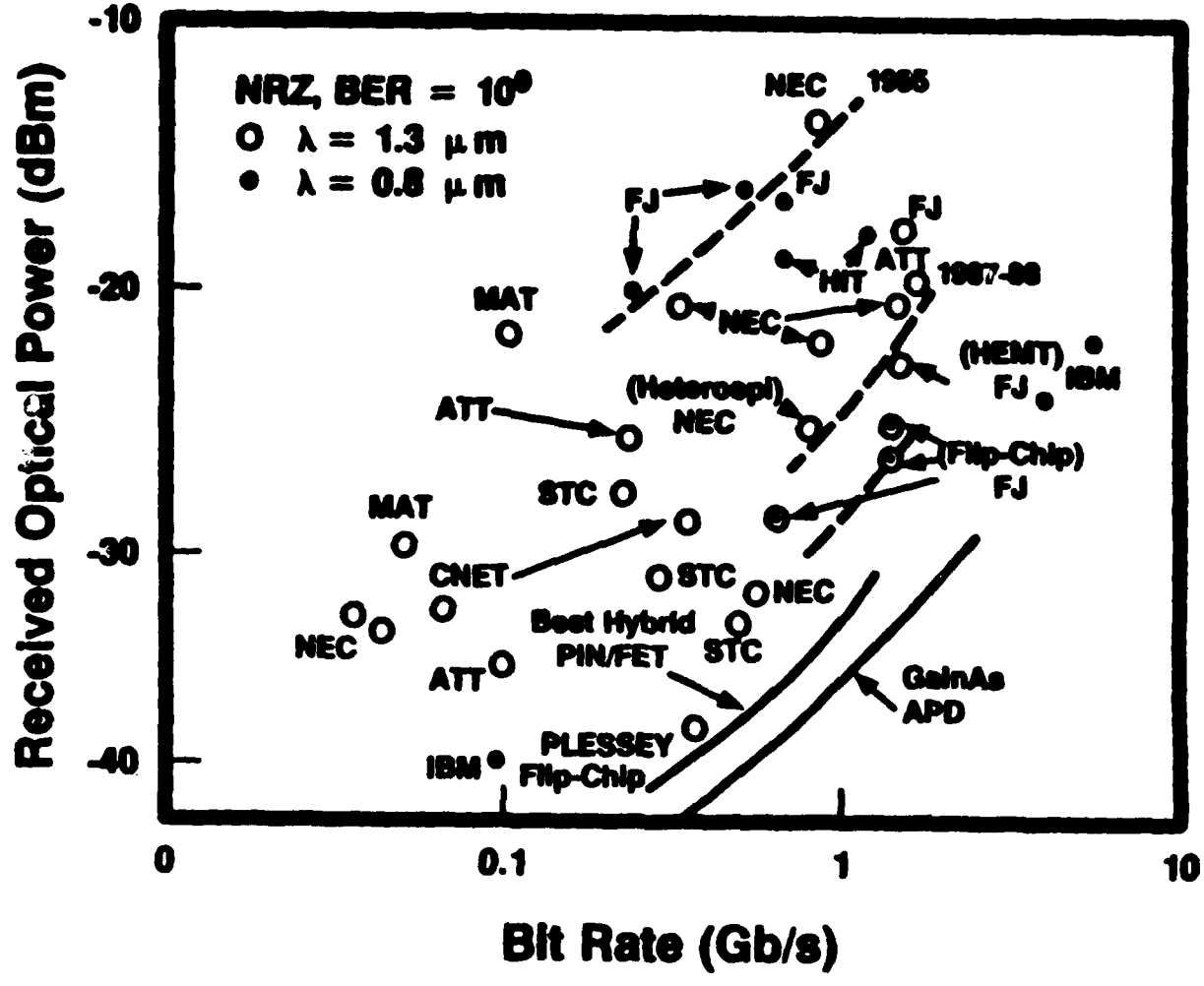


Figure 25

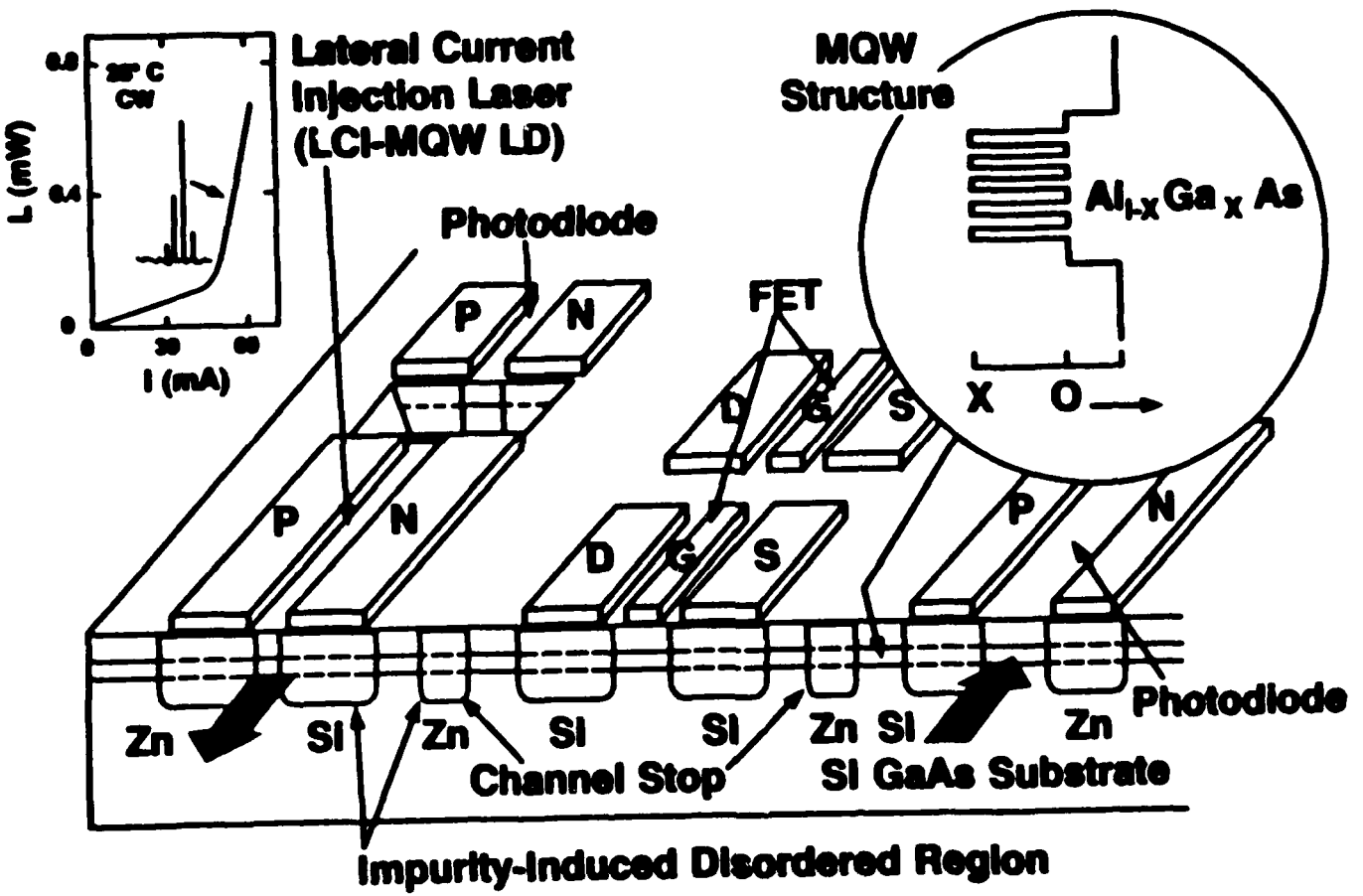

Lateral Current
Injection Laser
(LCI-MQW LD)
MQW
Structure
Photodiode
FET
P
N
D
G
S
X
O
Zn
Si
Channel Stop
Si GaAs Substrate
Impurity-Induced Disordered Region

Figure 26

III-V INTEGRATED OPTOELECTRONICS WORKSHOP

MARCH 28-30, 1989

MARINER'S INN, HILTON HEAD, SOUTH CAROLINA

Professor I. Adesida
University of Illinois
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